THE GAME TREE

OPERATOR'S MANUAL

PSE

THE GAME TREE

by PSE

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CONT.

INTRODUCTION

Game Tree is a completely solid state video game which utilizes state of the art semiconductor components. The game display and logic sequence are generated by three printed circuit boards. A 23 inch video monitor displays the game picture, and an advanced sound generation system adds realistic sounds to complete the environment.

Game Tree is a game for one player, who controls a realistic hunting rifle. Points are scored by shooting the target animals, while successfully avoiding the hunting dog.

In this manual, you will find a description of the game sequence of play and an explanation and location of all game adjustments. There are sections detailing the logic of the game and providing trouble-shooting assistance in case of problems.

GAME OPERATION

I. POWER ON. After an initial warm-up period, the game display will appear on the screen.

A. The squirrel, rabbit, turkey and the dog images will appear and move in a random fashion.
   1. The squirrel will run randomly across the foreground, up and down both trees or leap across from tree to tree.
   2. The rabbit will appear randomly in one of the six holes in the log and in the foreground.
   3. The turkey or dog will appear randomly and run randomly between the two trees.

B. High score, timer and player's score are displayed at the top of the screen.

C. The words "Game Over" will be displayed below the high score.

II. GAME START. Credit is established by inserting one coin (see game adjustments section for 2 coin credit).

A. The time will be set to 100 and begin counting down.

B. The players score will be set to 00000.

C. The words "Game Over" will disappear from the display.

D. Game sounds will be evident; including birds chirping, shot, hit and penalty audio.

III. GAME ACTION. The hunting gun can be positioned, aimed, and fired by the player.

A. Aim and fire the gun to hit the animals. A small shot explosion will appear on the screen when the gun is fired.

B. If a target is hit, the point value for that target will be displayed for a short time. A bell audio will ring with every hit.

C. If the hunting dog is hit 500 points will be subtracted from the players score, a penalty bell will sound and the dog will run quickly behind a tree.

D. The game proceeds until the timer reaches 000. The timer then stops, and if the player's score exceeds the high score, the new high score will be displayed.

GAME TREE MAJOR SECTIONS

A. POWER SUPPLY. The power supply for this board produces regulated +5 and regulated -12. The line voltage is applied to the primary of the power transformer through a line voltage selection switch. The secondaries of the transformer produce 8.5 vac and 26 vac center tapped.

The 8.5 VAC is full wave rectified by the 5 volt rectifier. The unregulated +10v is filtered by a 9,000 uF capacitor and regulated down to +5 volts by the 2N3055 power transistor which is heat sinked on the rear of the card guide. The base of the 2N3055 is controlled by a 741 op AMP which is Zener diode referenced to supply a stable 5 volt supply.

The 26 VAC is full wave rectified by the 12 volt bridge to produce -23VDC. A 100 uF capacitor filters the - supply which is then regulated down to -12VDC by a LM320T-12 voltage regulator. A 9600 uF capacitor filters the +supply which is then regulated down to +12VDC by a LM 340T-12 voltage regulator.

B. LOGIC BOARDS. Refer to game logic sections for a detailed explanation.

1. Board 1: Board 1 produces all the timing signals for the game. SYNC, horizontal and vertical counters and program control are also on Board 1.

2. Board 2: Board 2 is responsible for generating all the game images. Image locations, motion, and collisions also involve Board 2 circuitry.

3. Board 3: Board 3 contains the coin in, timer, audio, and shot generation circuitry.

C. CALIBRATION PANEL

1. The calibration panel has 5 pots and a slide switch. 4 pots are used to set the top, bottom, left and right shot boundies. The slide switch will switch on a calibration display for aligning the shot. The fifth pot is for setting the game volume.

D. WIRING HARNESS Refer to wiring harness diagram. The game contains two separate harnesses.

1. Power Harness: This harness provides interconnects between the line cord, line voltage select switch, power transformer, and monitor.

2. Main Harness: This harness provides interconnects between the motherboard, speakers, coin door components, calibration panel, hunting gun,

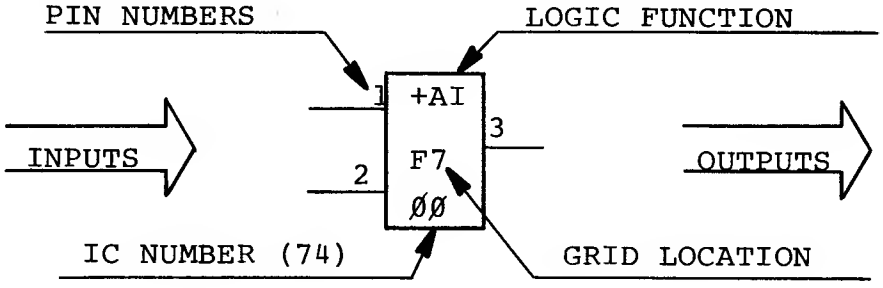
GAME LOGIC

INTRODUCTION

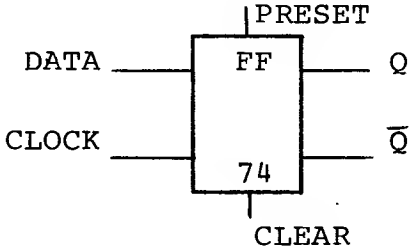
The P.C. boards are accessible through the front door of the cabinet. To facilitate identification of integrated circuits, a grid system of letters and numbers is marked on each board. The grid system of identification is marked on the circuit element on the schematics. The 7400 series logic identification has been abbreviated by deletion of the 74; e.g. "85" refers to a 7485.

The logic gates are drawn as boxes instead of logic symbols on the schematics. This system allows for fast and accurate troubleshooting. The inputs come in on the left side of the box, and the output leaves from the right side. A 2 digit number and letter in a box is the grid location on the P.C. board. The polarity and letters in the box refer to the gate's logic function; e.g. +AI tells you that the gate is performing a positive AND-INVERT logic function. The following symbols are used to represent standard logic functions:

+ positive true logic
- negative true logic
A AND
I invert
0 OR
⊕ exclusive OR
FF flip flop
LTCH latch



D type flip flops are drawn with this standard format.



THEORY OF OPERATION

Game Tree utilizes PSE's high speed processing technique. The game is programmable, that is, all game functions are controlled through a central processing section. This processing section is found on Board 1. The system operates in a similar manner as a microprocessor chip.

BOARD 1

The computer program for the game is held in the two PROMS on board 1, (location E2 and D2). Three four bit binary counters (L3, K3, J3) form the program counter which addresses the PROMS. The instruction address appears on Data Bits 1-16. Two 74154's (E4, D4) decode the instruction to produce the appropriate strobe. The strode signal is a pulse approximately 300 nano-seconds long. Each of the 32 strobes controls a part of the hardware circuitry.

B2 and B4 (8130's) compare the Prom data with bit and line address to synchronize the program with the real time T.V. display. These comparators are mainly used to display the scores.

The score valves are stored in a 16 X 4 RAM (L8). (See score RAM data table) This RAM is addressed by a 74193 (K8). The value in the RAM is decoded into the 7 segment format by a 7448 (J7). Each segment is selected for display by the 3-4 bit latches (F7, E7, D7). The 74151 (H7) selects and inputs the appropriate segment on the video line for display. The 74193 (K7) is used to add or subtract from the score values. The 7485 (L7) is used to compare scores to enable high score and game over functions to operate.

Sheet 2 schematic of board 1 contains drawings of the sync circuitry and bit and line counters.

BOARD 2

The board 2 circuitry generates the images for the game. The computer program which operates on board 1 controls the image locations on the screen.

There are 4 16 X 4 RAMs on board 2 organized to produce a 16 X 16 RAM memory. The program loads the appropriate image location in the correct RAM address. (See image RAM data sheet.)

The RAMs are addressed by a 74193 (F3). A random logic circuitry scans through the address in the RAMs for a given image. A line start pulse can be produced. This pulse occurs on the first line on which the image is to be displayed. This pulse sets a flip flop (H4, J1), which enables the image generation circuitry.

The 4 74s200 RAMs are organized to produce a memory array of 256 words by bits. Each of these 4 RAMs control the horrizontal location of an image. The bit address for the image on that level is loaded in the RAM. The entire RAM is cleared during vertical drive. For example, if an image is to appear at bit address 128, the program takes the bit address for that image (128) out of the 16 X 4 RAMs (E2, E3, D2, D3), and addresses the 256 X 4 RAMs to that location (128). A one (1) is written into that location. During display, the 256 X 4 RAMs are addressed directly from the bit counters. When a logic 1 appears out of RAM, it is channeled and selected through the 74279 (A11), and produces a bit start pulse.

There are two image prom circuits for this game. Prom 1 (F12, F14) contains the squirrel and squirrel point value. Prom 2 (E12, E14) contains the other targets and point values. The 74161 (G10) and 7474 (E9) creates the bit address for the image. Ten 7486's (E11, F11, G11) can invert the bit or line address to change the direction that the image faces. The 74151 (D14) converts the 8 bit image word into serial form for video display.

The Prom 2 (L1) circuit is the same as the Prom 1 circuit, except that there are no 7486's to invert the line address.

Image motion is carried out under program control. Two 7483 (D4, D7) 4 bit adders add the image address to the speed number every frame to move the image. Two 7485's (D5, D6) can compare the locations of the images to determine the boundries that the images may move in. A 74164(D1) shifter is clocked off P.C. clock to produce a random bit. The program will look at this bit for all random image actions. The 32 X 8 PROMS's (A2, A3) contains PROM address codes and image speeds. Each has its own speed and address block in the image PROM.

There are two 74150's (G1, F1) on board 2. The program controls this circuit so that any of the 32 input lines, or CONDITIONS, can be selected down to one COND. out line. Conditions are inputs to the program. By sensing these outputs (conditions 16-23), the program is able to switch to appropriate images.

BOARD 3

Board 3 contains coin-in, shot generation, and audio circuitry. The coin switch gets debounced by the two 7400 (A4) gates. The output of this latch configuration triggers a 74123 (A3) one shot.

The output of the 74123 clocks a 7474 flip flop (B4), providing the coin-in signal is still present. The 2nd half of the 7474 is used to count two coins. The coin-in signal is clocked through a 7474 (B6) to initialize the game for proper score and image display. A switch will select one or two coins through a 7400 (B3) multiplexer circuit. The selected credit signal is applied to one input

of a 7400 latch. When the start switch is pressed, the latch is set, and a game-on condition exists. The program will generate a strobe 30 when the timer is at 000 to reset the coin-in flip flops and end the game. A 74123 (A3) is used as a power on reset (POR). When power is applied, the one shot will fire and condition 9 will reset the game.

The shot circuitry generates the small shell explosion image and positions this image on the screen. A transistor circuitry generates a constant current ramp. This ramp is compared to the H location voltage. The horizontal position put on the gun axis varies from 1.5 to 2.5 volts. The LM339 (A11) comparator output latches the 74174 (A5) latch. The 7485 comparator (B5) generates the horizontal shot position. The vertical position portion is identical in concept to the horizontal position circuitry. The 7485 comparator (B8) output generates the vertical window. ANDing the vertical and horizontal windows generates an 8 bit by 8 line shot window. 7486's and 7402's (A7, B7) generate the shell explosion image.

The game time uses an NE555 (D5) timer chip in a one shot configuration. The program senses condition 6 every frame. When this condition goes high, the program decrements the timer value by 1, and retriggers the NE555 with strobe 28. The time adjustment switch determines the length of the NE555's output pulse.

AUDIO

The bird chirping sound effects are generated by 2 separate circuitries. This sound is controlled by two 74161's which at appropriate counts, switch on and off a NE555 to create the chirping effect.

The shot audio is created by shaping the noise output of two 74164 shift resistors. The shaping is controlled by a MC3340 linear attenuator.

The penalty and hit bells are generated by controlling the amplitude of a 566 VCO. Two 74123 one shots, (B4, B5) control the starting of the bell sounds.

The various audio sounds are mixed through resistors into two separate LM380 push-pull audio amplifiers which will provide at least six watts of power per channel. Two MC3340 Linear Attenuators control the volume.

RIFLE ASSEMBLY DESCRIPTION

RIFLE ASSEMBLY

The rifle on Game Tree is installed on a shaft which is mounted in a steel collar on the flat surface of the cabinet. A smaller shaft goes inside the main shaft and a pin passes through both shafts to hold them together. The outer shaft has a slot instead of a hole for the pin, allowing the inner shaft to turn sideways.

The up and down motion is provided by a second pin in the inner shaft. A bracket pivots up and down on the second pin and the rifle stock is bolted to the top bracket. The trigger is also mounted on this bracket. Two gear driven pots are installed with spring brackets to keep meshing gear under tension. This whole assembly is enclosed by a plastic cover.

RIFLE REMOVAL

Reaching in from the front door, remove C. clip from the main shaft on the rifle. Disconnect the molex connector from the main harness and lift the rifle and main shaft straight up. For installation, reverse procedure.

SIGHT CALIBRATION

Install rifle on the game and connect it to the main harness and calibration board. Turn the switch on the calibration board so that the cross hair appears on the screen. Turn each pot to the limit on the calibration board marked Top, Bottom, Left, and Right so that the cross hair is at the limit. In other words, the pot marked Top should be turned so that the horizontal cross hair is at maximum upper limit, turn the Bottom pot so that horizontal cross hair is at the bottom limit. The procedure is the same for Left and Right. Aim the rifle at the center of the screen. For side to side calibration, follow the steps listed below:

1. Lift the pinion away from the meshing gear on the side to side pot on the rifle assembly and turn until the vertical cross hair is lined up with the rifle sight.
2. Release the pinion and make sure it meshes properly with the gear.
3. Turn the rifle all the way to the right and adjust the Right pot on the calibration board until the vertical cross hair lines up with the rifle sight.
4. Turn the rifle all the way to the left and realign the rifle sight and cross hair using Left Cal pot. Again, turn the rifle to the right and readjust Right pot.
5. Repeat steps 3 and 4 until vertical cross hair tracks the rifle sight.
6. For up and down adjustment follow the steps above using up, down calibration pots and vertical pot on the rifle.

ADJUSTMENTS

I. AUDIO VOLUME

A. Gain access to the calibration panel through the coin door.
B. Adjust the control marked volume for the desired game volume.
C. Do not adjust any of the other controls or gun misalignment will occur.

II. GUN ALIGNMENT

A. Gain access to the calibration panel through the coin door.
B. Set the slide switch to the CAL. DISPLAY position. This will produce a shot alignment display on the screen.
C. There are four calibration controls on the panel. These controls set the top, bottom, left, and right shot alignments. Adjust them as follows:
   1. Aim the gun to the right side of the screen. Adjust the control labled right so that the Cal Display is in line with the gun.
   2. Aim the gun to the left side of the screen. Adjust the control labeled left so that the Cal Display is in line with the gun.
   3. Aim the gun to the top of the screen and align the Cal Display by adjusting the control labeled Top.
   4. Aim the gun to the bottom of the screen and align the Cal Display by adjusting the control labeled Bottom.
D. Slide the Cal Display Switch to the off position.

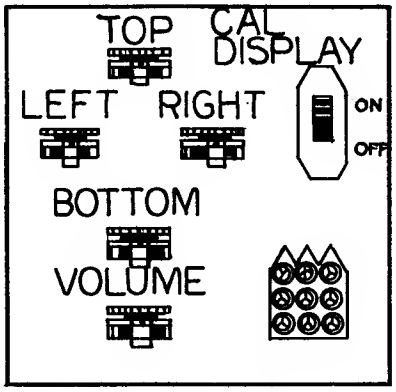
III. LENGTH OF GAME

A. Earlier models of Game Tree have a three (3) position slide switch for length of game selection. This switch is located at the top left of board 3. Game time is selectable to 60, 90, or 120 seconds by positioning the switch to the left, center or right respectively.
B. Later models of Game Tree have a Dip Switch for game time selection. This switch is located at the top left of board 3. Game time is selectable to 60, 90 or 120 seconds by sliding the appropriate switch to the "ON" position.

IV. 2 COIN CREDIT

A. Earlier models of Game Tree incorporate a slide switch for credit selection. This switch is located at the top left of board #3, and is to the left of the Game Time Switch. Slide the switch to the left for one (1) coin credit, or to the right for two (2) coin credit.

B. Later models incorporate a dip switch for credit selection. This switch is located at the top left corner of board #3. Slide the switch marked "2 Coin" to the "on" position if 2 coin credit is desired.



CALIBRATION DISPLAY BOARD

TABLES AND REFERENCES

IMAGE RAM DATA (E2, E3, D2, D3)

ADDRESS	RAM BITS 1 2 3 4 5 6 7 8	RAM BITS 9 10 11 12 13 14 15 16
0	SQUIRREL BIT ADDRESS	NOT USED
1	RABBIT BIT ADDRESS	
2	TURKEY/DOG BIT ADDRESS	
3	(NOT USED)	
4	SQUIRREL LINE ADDRESS	IMAGE # / LINE INVERT / BIT INVERT / (NOT USED)
5	RABBIT LINE ADDRESS	
6	TURKEY/DOG LINE ADDRESS	
7	(NOT USED)	
8	SQUIRREL IMAGE #	NOT USED
9	SQUIRREL PAUSE COUNT	
10	RABBIT PAUSE COUNT	
11	RABBIT RANDOM COUNT	
12	DOG/TURKEY IMAGE #	
13	DOG/TURKEY PAUSE COUNT	
14	DOG/TURKEY DIRECTION	
15		

TABLES AND REFERENCES

IMAGE PROM ADDRESS MAP

GT1A

IMAGE #	DESCRIPTION	ADDRESS
0	SQUIRREL → LEGS APART	000-127
1	SQUIRREL ↑ LEGS APART	128-255
2	SQUIRREL ↗ LEGS APART	256-383
4	200 POINTS	384-511

GT1B

0	SQUIRREL → LEGS TOGETHER	000-127
1	SQUIRREL ↑ LEGS TOGETHER	128-255
3	SQUIRREL ↘ LEGS APART	256-383
4	500 POINTS	384-511

GT2A

0	RABBIT EARS APART	000-127
1	TURKEY LEGS APART	128-255
2	DOG LEGS APART	256-383
3	400 POINTS	384-511

GT2B

0	RABBIT EARS TOGETHER	000-127
1	TURKEY LEGS TOGETHER	128-255
2	DOG LEGS TOGETHER	256-383
4	300 POINTS	384-511

EDGE CONNECTOR PIN INDEX

BOARD 1

1.	GROUND	A.	GROUND
2.	+5	B.	+5
3.	BIT ADDRESS 2	C.	BIT ADDRESS 1
4.	+12	D.	+12
5.	BIT ADDRESS 4	E.	BIT ADDRESS 3
6.	BIT ADDRESS 6	F.	BIT ADDRESS 5
7.	BIT ADDRESS 8	H.	BIT ADDRESS 7
8.	-STROBE	J.	ADDRESS BIT START
9.	-STROBE 17	K.	-STROBE 16
10.	-STROBE 19	L.	-STROBE 18
11.	-STROBE 21	M.	-STROBE 20
12.	-STROBE 23	N.	-STROBE 22
13.	-STROBE 25	P.	-STROBE 24
14.	-STROBE 27	R.	-STROBE 26
15.	-STROBE 30	S.	-STROBE 28
16.	-STROBE 31	T.	-STROBE 31
17.	CONDITION 27	U.	DATA BIT 16
18.	DATA BIT 15	V.	DATA BIT 14
19.	DATA BIT 13	W.	DATA BIT 12
20.	DATA BIT 11	X.	DATA BIT 10
21.	PC CLOCK	Y.	DATA BIT 8
22.	DATA BIT 7	Z.	DATA BIT 6
23.	DATA BIT 5	a.	DATA BIT 4
24.	DATA BIT 3	b.	DATA BIT 2
25.	DATA BIT 1	c.	LINE ADDRESS 1
26.	LINE ADDRESS 2	d.	LINE ADDRESS 3
27.	LINE ADDRESS 4	e.	LINE ADDRESS 5
28.	LINE ADDRESS 6	f.	LINE ADDRESS 7
29.	LINE ADDRESS 8	h.	ADDRESS LINE START
30.	-H DRIVE	j.	READ EXTERNAL ADDRESS
31.	H. RESET	k.	H CLOCK
32.	-V DRIVE	l.	COMPOSITE BLANK
33.	DATA BIT 9	m.	+H DRIVE
34.	+STROBE A	n.	IMAGE CLOCK
35.	+ V DRIVE	p.	CONDITION OUT
36.	CONDITION 8	r.	CONDITION 7
37.	-BIT COMPARE	s.	INHIBIT
38.	V. CLOCK	t.	- LINE COMPARE
39.	VIDEO	u.	INTERLACE
40.	-12	v.	-12
41.	RAM BIT 12	w.	CONDITION 25
42.	+5	x.	+5
43.	GROUND	y.	GROUND

EDGE CONNECTOR PIN INDEX CONT.

BOARD 2

1.	GROUND	A.	GROUND
2.	+5	B.	+5
3.	BIT ADDRESS 2	C.	BIT ADDRESS 1
4.	+12	D.	+12
5.	BIT ADDRESS 4	E.	BIT ADDRESS 3
6.	BIT ADDRESS 6	F.	BIT ADDRESS 5
7.	BIT ADDRESS 8	H.	BIT ADDRESS 7
8.		J.	ADDRESS BIT START
9.		K.	STROBE 16
10.	STROBE 19	L.	STROBE 18
11.	STROBE 21	M.	STROBE 20
12.	STROBE 23	N.	STROBE 22
13.	STROBE 25	P.	STROBE 24
14.	STROBE 27	R.	STROBE 26
15.	STROBE 30	S.	STROBE 28
16.	STROBE 31	T.	CONDITION 0
17.	CONDITION 27	U.	CONDITION 10
18.		V.	CONDITION 1
19.	DATA BIT 13	W.	
20.	DATA BIT 11	X.	DATA BIT 10
21.	P.C. CLOCK	Y.	DATA BIT 8
22.	DATA BIT 7	Z.	DATA BIT 6
23.	DATA BIT 5	a.	DATA BIT 4
24.	DATA BIT 3	b.	DATA BIT 2
25.	DATA BIT 1	c.	LINE ADDRESS 1
26.	LINE ADDRESS 2	d.	LINE ADDRESS 3
27.	LINE ADDRESS 4	e.	LINE ADDRESS 5
28	LINE ADDRESS 6	f.	LINE ADDRESS 7
29.	LINE ADDRESS 8	h.	ADD LINE START
30.	-H DRIVE	j.	SHOT OUTPUT
31.	H. RESET	k.	H CLOCK
32.	-V DRIVE	l.	COMPOSITE BLANK
33.	DATA BIT 9	m.	H DRIVE
34.	+STROBE A	n.	
35.	+V DRIVE	p.	CONDITION OUT
36.	CONDITION 8	r.	CONDITION 7
37.	PENALTY	s.	CONDITION 9
38.	V CLOCK	t.	CONDITION 6
39.	VIDEO	u.	
40.	-12	v.	-12
41.		w.	CONDITION 25
42.	+5	x.	+5
43.	GROUND	y.	GROUND

EDGE CONNECTOR PIN INDEX CONT.

BOARD 3

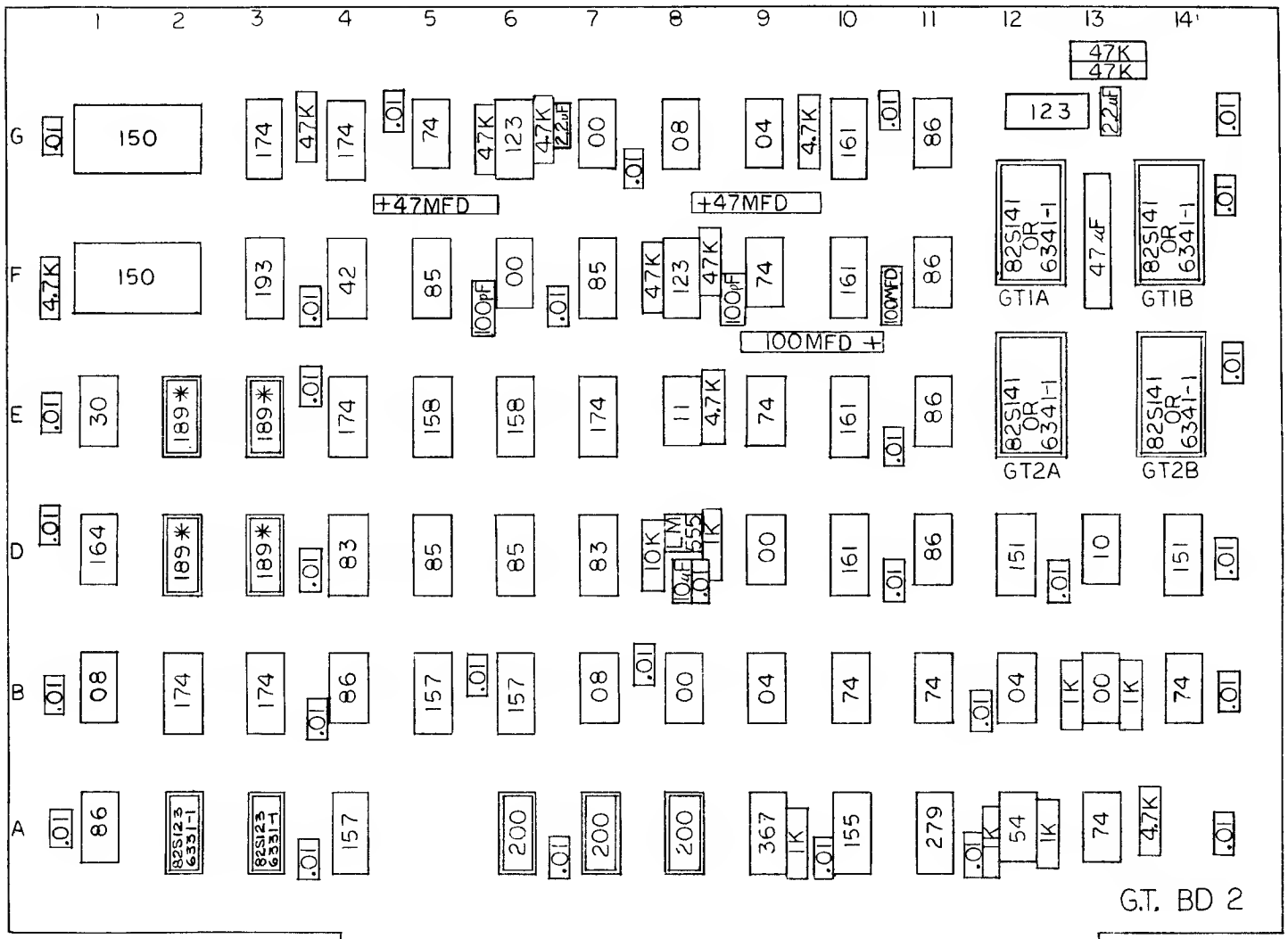
1.	GROUND	A.	GROUND
2.	+5	B.	+5
3.	BIT ADDRESS 2	C.	BIT ADDRESS 1
4.	+12	D.	+12
5.	BIT ADDRESS 4	E.	BIT ADDRESS 3
6.	BIT ADDRESS 6	F.	BIT ADDRESS 5
7.	BIT ADDRESS 8	H.	BIT ADDRESS 7
8.		J.	ADDRESS BIT START
9.		K.	STROBE 16
10.	H LOCATION	L.	CH. 1 AUDIO A
11.	V LOCATION	M.	
12.	STROBE 23	N.	COIN SWITCH N.C.
13.	COIN SWITCH N.C.	P.	STROBE 24
14.		R.	STROBE 26
15.	STROBE 30	S.	STROBE 28
16.		T.	CONDITION 0
17.	HIT	U.	CONDITION 10
18.	VOL. I	V.	CONDITION 1
19.		W.	CONDITION 9
20.	P.C. CLOCK	X.	FIRE SWITCH
21.		Y.	
22.	DATA BIT 7	Z.	DATA BIT 6
23.	DATA BIT 5	a.	DATA BIT 4
24.	DATA BIT 3	b.	DATA BIT 2
25.	DATA BIT 1	c.	LINE ADDRESS 1
26.	LINE ADDRESS 2	d.	LINE ADDRESS 3
27.	LINE ADDRESS 4	e.	LINE ADDRESS 5
28.	LINE ADDRESS 6	f.	LINE ADDRESS 7
29.	LINE ADDRESS 8	h.	SHOT CAL SWITCH
30.	-H DRIVE	j.	SHOT OUTPUT
31.	VOL. II	k.	CH. 2 AUDIO (B)
32.	-V DRIVE	l.	COMPOSITE BLANK
33.	TRIAC CONTROL	m.	+H DRIVE
34.	CH. 2 AUDIO (A)	n.	
35.	+V DRIVE	P.	
36.		r.	
37.	CONDITION 30	s.	CONDITION 9
38.		t.	CONDITION 6
39.	VIDEO	u.	INTERFACE
40.	-12	v.	-12
41.	CH. 1 AUDIO (B)	w.	CONDITION 25
42.	+5	x.	+5
43.	GROUND	y.	GROUND

STROBES

0.	DISPLAY CONDITIONS AND SEGMENTS	16.	LOAD CONDITION
1.	LOAD SCORE RAM ADDRESS	17.	
2.	ADVANCE RAM ADDRESS	18.	WRITE RB 1-8
3.	LOAD SCORE UPDATE COUNTER	19.	WRITE RB 9-16
4.	RESET SCORE UPDATE COUNTER	20.	CLR SCORE LATCH
5.	WRITE SCORE RAM	21.	ADV. RAM
6.	ADVANCE SCORE UPDATE COUNTER	22.	CLOCK UPDATE F/F
7.	CARRY CLEAR	23.	LATCH IMAGE #
8.	TRANSFER CARRY	24.	LATCH RAM IN BITS 1-8
9.	ADVANCE UPDATE COUNTER	25.	LOAD RAM ADDRESS
10.	LOAD DOWN COUNTER	26.	CLR COLLISION ON TRACK
11.	DECREMENT DOWN COUNTER	27.	LOAD DISPLAY RAM
12.	LOAD P.C. IF D ≠ 0	28.	TRIGGER TIMER/AUDIO/BLANK
13.	LOAD P.C. IF D = 0	29.	(NOT AVAIL.)
14.	WRITE REGISTER X	30.	GAME OVER
15.	JUMP TO REGISTER X	31.	NOT USABLE

GAME TREE CONDITIONS

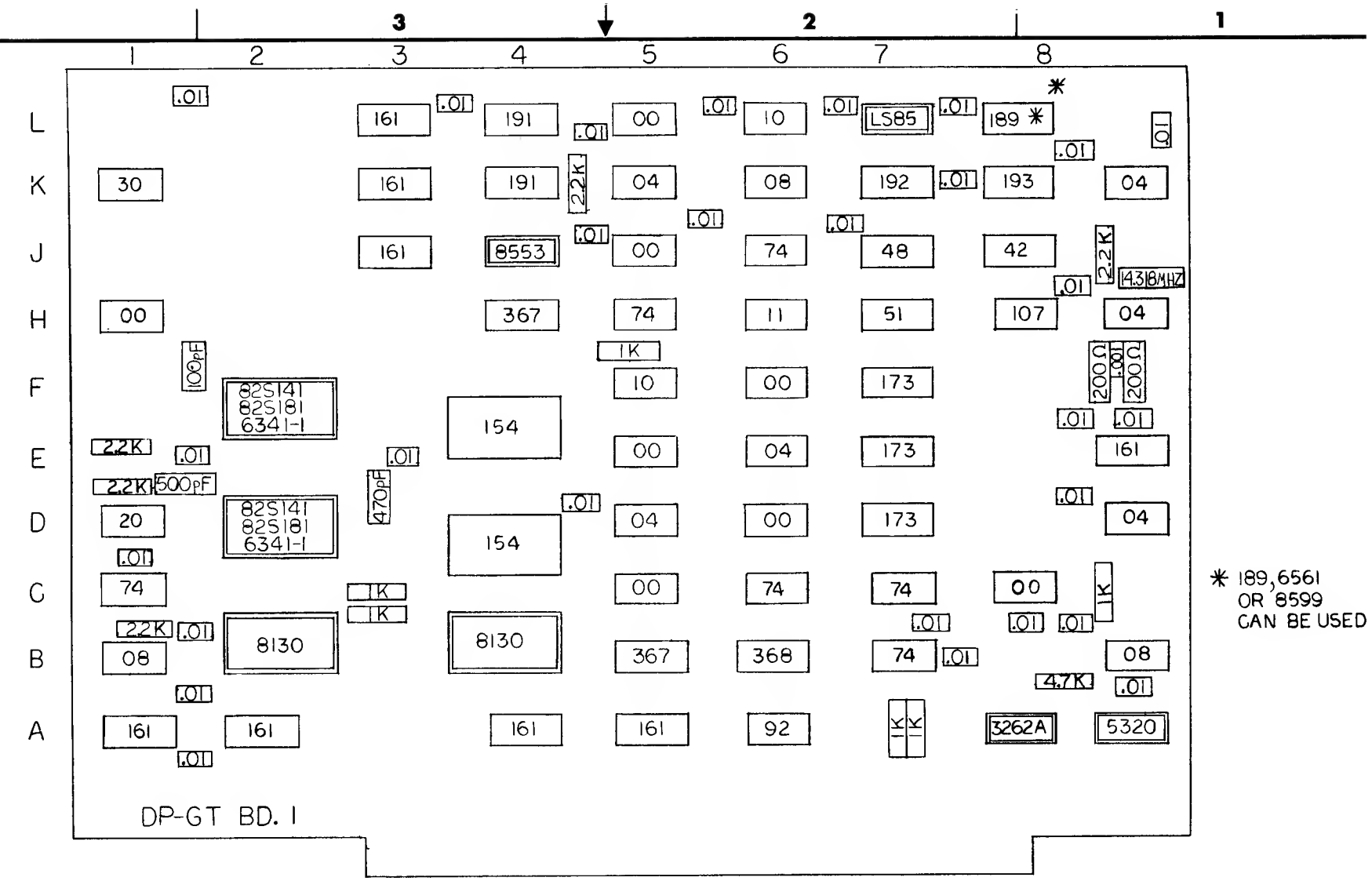
0.	COIN IN INITIALIZE	16.	P2 SCORE IMAGE
1.	CLEAR HIGH SCORE	17.	P2 RESET IMAGE
2.	RABBIT HIT	18.	
3.	TURKEY HIT	19.	
4.	DOG HIT	20.	
5.	(P2 HIT)	21.	
6.	UPDATE TIME	22.	
7.	A<B SCORE	23.	
8.	A>B SCORE	24.	
9.	POR INITIALIZE	25.	A=B SCORE
10.		26.	
11.	END OF TRAVEL A=B	27.	
12.		28.	RAM A>B DATA
13.	(P2 HIT)	29.	RAM A<B DATA
14.	(P2 HIT)	30.	P2 SCORE
15.	RANDOM CONDITION	31.	P1 SCORE



* 189, 6561 OR 8599 CAN BE USED.

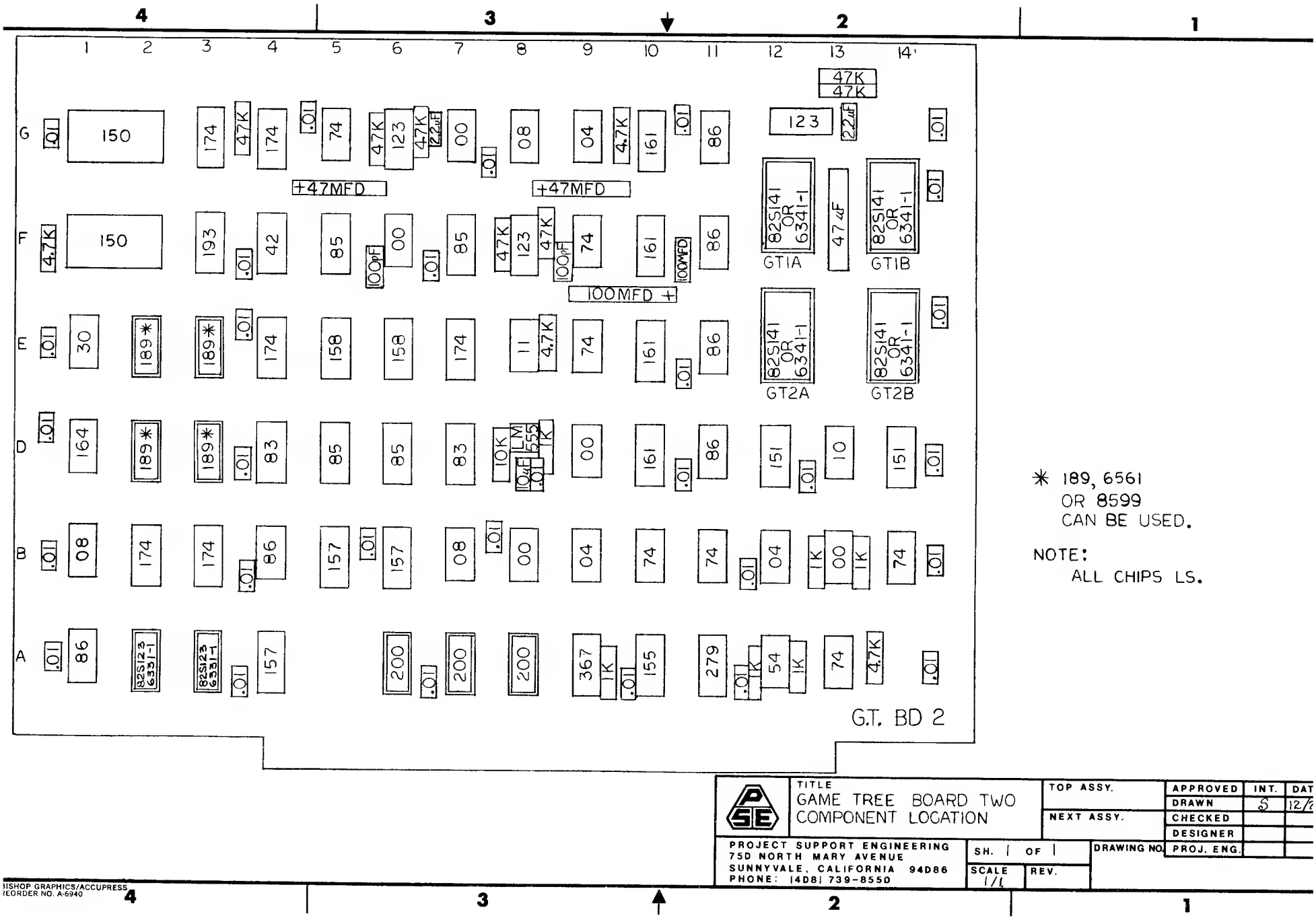
NOTE:
ALL CHIPS LS.

PSE	TITLE: GAME TREE BOARD TWO COMPONENT LOCATION	TOP ASSY.	APPROVED	INT.	DAT
		NEXT ASSY.	DRAWN	S	12/
			CHECKED		
			DESIGNER		
PROJECT SUPPORT ENGINEERING 750 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 739-8550		SH. 1 OF 1	DRAWING NO.	PROJ. ENG.	
		SCALE 1/1	REV.		



NOTE:
ALL CHIPS LS.

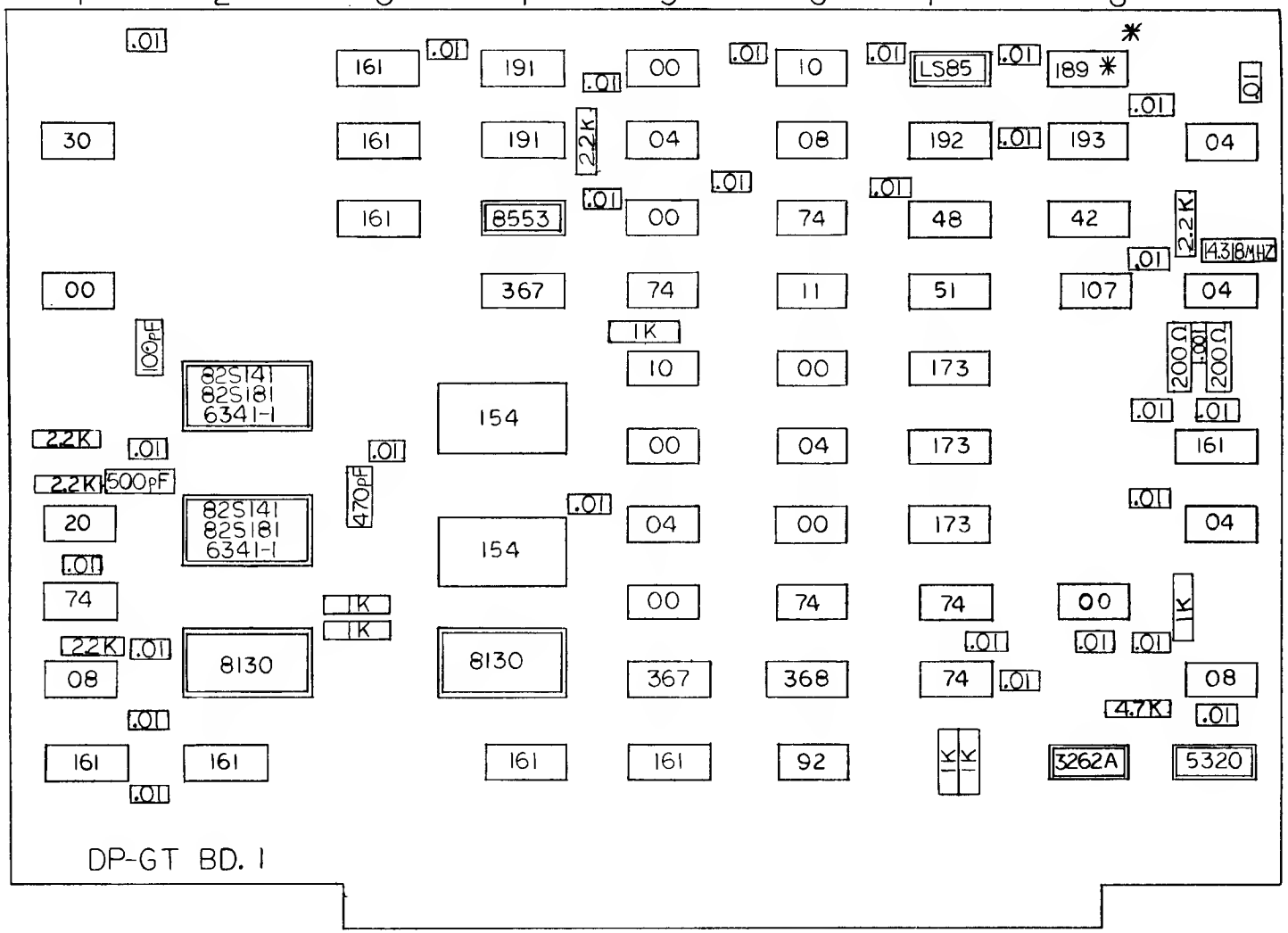
PSE	TITLE: DESERT PATROL & GAME TREE COMPONENT LOCATION BOARD 1	TOP ASSY.	APPROVED	INT.	DAT
		NEXT ASSY.	DRAWN	J	12/7
			CHECKED		
			DESIGNER		
PROJECT SUPPORT ENGINEERING 750 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 739-8550		SH. 1 OF 1	DRAWING NO.	PROJ. ENG.	
		SCALE 1/1	REV.		



* 189, 6561 OR 8599 CAN BE USED.

NOTE:
ALL CHIPS LS.

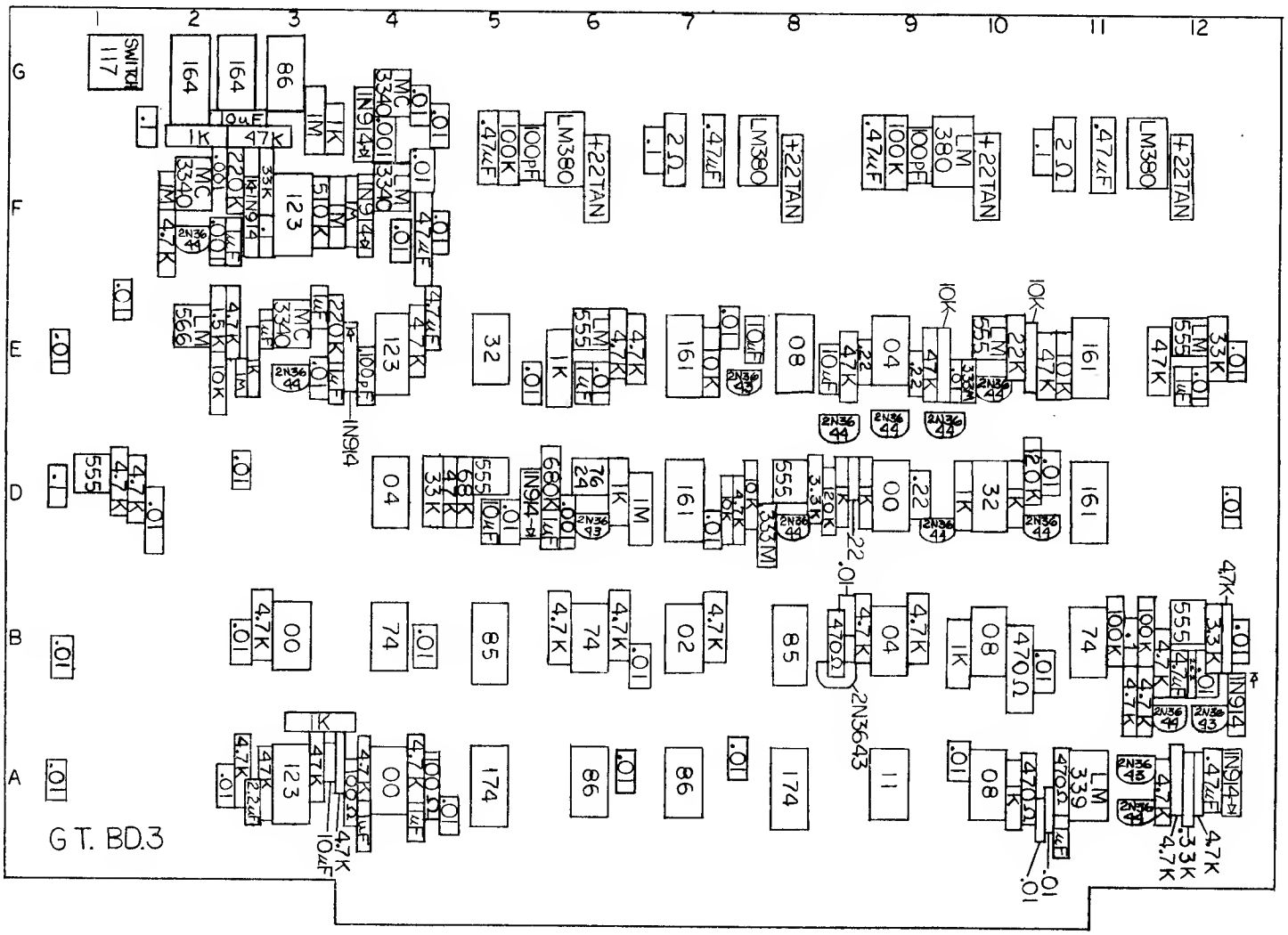
PSE	TITLE: GAME TREE BOARD TWO COMPONENT LOCATION	TOP ASSY.	APPROVED	INT.	DAT
		NEXT ASSY.	DRAWN	S	12/
			CHECKED		
			DESIGNER		
PROJECT SUPPORT ENGINEERING 75D NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 739-8550		SH. 1 OF 1	PROJ. ENG.		
		SCALE 1/1	REV.	DRAWING NO.	



* 189, 6561 OR 8599 CAN BE USED

NOTE:
ALL CHIPS LS.

PSE	TITLE: DESERT PATROL & GAME TREE COMPONENT LOCATION BOARD 1	TOP ASSY.	APPROVED	INT.	DAT
		NEXT ASSY.	DRAWN	JB	4/7
			CHECKED		
			DESIGNER		
PROJECT SUPPORT ENGINEERING 750 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94088 PHONE: (408) 739-8550	SH. 1 OF 1	DRAWING NO.	PROJ. ENG.		
	SCALE 1/1	REV.			



NOTE:
ALL I.C.'S LS.

PSE	TITLE: GAME TREE BOARD THREE COMPONENT LOCATION	TOP ASSY.	APPROVED	INT.	DATE
		NEXT ASSY.	DRAWN	S	12/7
			CHECKED		
			DESIGNER		
PROJECT SUPPORT ENGINEERING 750 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 739-8550		SH. 1 OF 1	DRAWING NO.	PROJ. ENG.	
		SCALE 1/1	REV.		

SHOP GRAPHICS/ACCUPRESS
ORDER NO. A-6940

GAME TREE PARTS LIST

PART NUMBER	DESCRIPTION	QUANTITY
01	EDGE DRESSER	1
02	TRIGGER ASSEMBLY	1
03	MAIN ASSEMBLY BRACKET	1
04	WASHER ¼" (LOCK)	2
05	#6-32 BUTTON HEAD SCREW	4
06	VERTICAL GEAR	1
07	5K POT	1
08	#6-32 BUTTON HEAD SCREW	2
09	KEEPER (WASHER)	1
10	HORIZONTAL POT BRACKET	1
11	STAR WASHER	1
12	HEX HEAD NUT	1
13	#4-40 SET SCREW	1
14	PINION GEAR	1
15	'C' RING	1
16	PIVOT PIN	1
17	INNER SHAFT	1
18	#4-40 MACHINE HEAD SCREW	2
19	HORIZONTAL GEAR	1
20	3/16" ROLL PIN	1
21	5K POT	1
22	¼"-20 NUT	2
23	VERTICAL POT BRACKET	1
24	PINION GEAR	1
25	HEX HEAD NUT	1
26	STAR WASHER	1
27	KEEPER (WASHER)	1
28	3/8" EXPANSION PIN	1
29	OUTER SHAFT	1
30	ASSEMBLY COVER	1
31	#6-32 BUTTON HEAD SCREW (BLK.)	4
32	FLAT WASHER (BLK.)	4
33	BARREL	1
34	#7 X 1¼" OVAL HEAD SCREW	2
35	REAR SIGHT CAP	1
36	RECEIVER PLUG	1
37	RIFLESTOCK	1
38	BUTT PLATE	1
39	#20 X 2" HANGER BOLT	2
40	#8 X 1¼" SLOTHEAD	2
41	#8 X 3/4" PH. PHIL. SMS. BLK.	2
42	TRIGGER GUARD	1
43	MOTHERBOARD	1
44	PC 1	1
45	PC 2	1
46	PC 3	1
47	LINE SELECT BOARD	1

GAME TREE PARTS LIST CONT.

PART NUMBER	DESCRIPTION	QUANTITY
48	CALIBRATION BOARD	1
49	CABINET	1
50	SPEAKER	2
51	SPEAKER COVER	2
52	BANNER	1
53	FRONT BEZEL	1
54	AMBER PLEX	1
55	FAN MOTOR	1
56	FAN BLADE	1
57	MONITOR BOARD	1
58	SCENERY BOARD	1
59	DECAL	1
60	FOOTSTEP	1
61	COIN DOOR	1
62	COIN DOOR LOCK	1
63	BACK PANEL LOCK	1
64	COUNTER	1
65	COIN BOX	1
66	INDICATOR LAMPS	2
67	LIGHT SOCKET	3
68	SOLENOID	1
69	2 WAY MIRROR	1
70	RIFLE SUPPORT CONE	1
71	TRANSFORMER BOARD	1
72	½" SHEET METAL SCREW	2
73	COIN ACCEPTOR	1
74	AC POWER CORD	1
75	VELCRO	1
76	1 LAMP	1
77	2N3055 TRANSISTOR	1
78	RCA 40347 TRANSISTOR	1
79	2N 3643 TRANSISTOR	1
80	2N 3644 TRANSISTOR	1
81	195-K-1 TRANSFORMER	1
82	52118 PULSE TRANSFORMER	1
83	1N 764 DIODE	1
84	1N 914 DIODE	7
85	1N 4001 DIODE	1
86	43 PIN EDGE CONNECTOR	3
87	36 PIN MALE PLUG	1
88	36 PIN FEMALE PLUG	1
89	POWER HARNESS	1
90	SIGNAL HARNESS	1
91	12 SMALL PIN MALE PLUG	2
92	12 SMALL PIN FEMALE PLUG	2
93	9 PIN MALE PLUG	1
94	9 PIN FEMALE PLUG	1

GAME TREE PARTS LIST CONT.

PART NUMBER	DESCRIPTION	QUANTITY
95	6 SMALL PIN MALE PLUG	1
96	6 SMALL PIN FEMALE PLUG	1
97	3 PIN MALE PLUG	2
98	3 PIN FEMALE PLUG	2
99	6 LARGE PIN MALE PLUG	2
100	6 LARGE PIN FEMALE PLUG	2
101	12 INLINE PLUG MALE	1
102	12 INLINE PLUG FEMALE	1
103	12 PIN MALE PLUG	1
104	12 PIN FEMALE PLUG	1
105	BRIDGE MDA 970-1	1
106	FUSE CLIP	1
107	SLIDE SWITCH	1
108	22K	1
109	2.2 UF	7
110	SPECIAL SLIDE SWITCH	1
111	FUSE 312003	1
112	FUSE 313125	1
113	12 PIN MOTOROLA PLUG MALE	1
114	9600 mF 25V	2
	I.C.'s	
115	74LS00	15
116	74LS04	12
117	74LS08	9
118	74LS10	3
119	74LS11	3
120	74LS30	2
121	74LS42	2
122	7454	1
123	74LS74	16
124	74LS83	2
125	74LS85	6
126	74LS86	9
127	74LS123	6
128	74LS151	3
129	74LS155	1
130	74LS157	3
131	74LS158	5
132	74LS161	12
133	74LS164	3
134	74LS174	8
135	74LS189	4
136	74LS193	1
137	74LS200	3

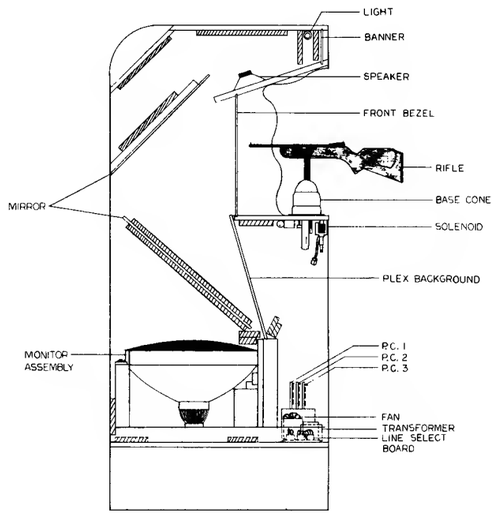
GAME TREE PARTS LIST CONT.

PART NUMBER	DESCRIPTION	QUANTITY
	I.C.'s CONT.	
138	74LS279	1
139	NE 555	8
140	74LS367	3
141	LM 339	1
142	74LS02	1
143	3340MC	5
144	74161	4
145	7400	1
146	74LS32	2
147	LM566	1
148	LM380	4
149	74LS20	1
150	74LS48	1
151	74LS92	1
152	74LS107	1
153	74154	2
154	74LS173	3
155	74LS191	2
156	74LS192	1
157	74LS193	1
158	DM8098	1
159	DM8130	2
160	DM8553	1
161	222	1
162	100uF	1
163	CRYSTAL 14.31818	1
164	470 CAP	1
	RESISTORS	
165	LM340T-12	1
166	DIODE IN914	7
167	470 ohm	4
168	2 ohm	2
169	1 Meg	5
170	1K	25
171	680	1
172	220K	2
173	510K	1
174	120K	2
175	100 ohm	2
176	1.5K	1
177	68K	1
178	10K	8

GAME TREE PARTS LIST CONT.

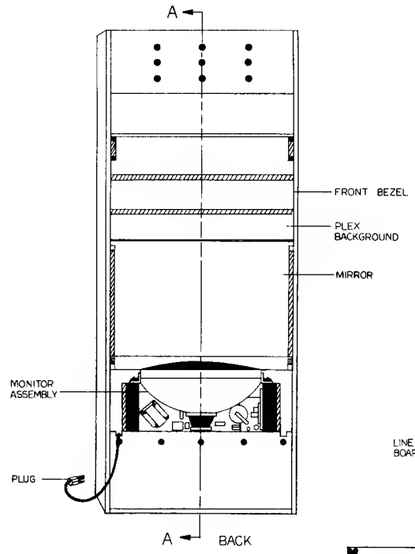
PART NUMBER	DESCRIPTION	QUANTITY
	RESISTORS CONT.	
179	3.3K	2
180	33K	5
181	47K	18
182	100K	4
183	4.7K	27
184	74150	2
185	74154	2
186	3262 ADC	1
187	LM741CN	1
188	LM320T-12	1
	CAPACITORS	
189	0.47uF 16V	5
190	2.2uF 50V	3
191	10uF 16V	6
192	.22K 100V	4
193	.1mf 50V	2
194	333mf 50V	2
195	.001uF 50V	4
196	100pF 1KV	4
197	.1 16V	5
198	.01	95
199	22 TANTALUM 16V	4
200	1uF 50V	10
201	47uF 16V	4
202	4.7 16V	2
203	TR3643	7
204	TR3644	11
205	560pF	1

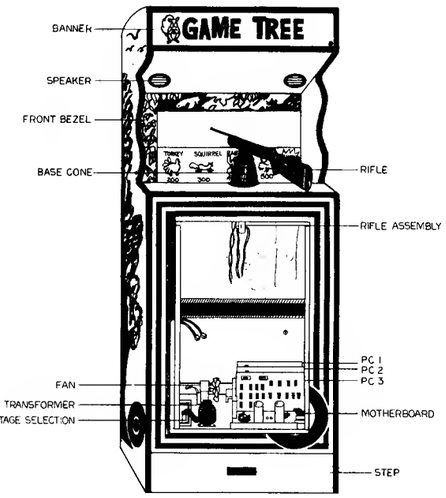
REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL



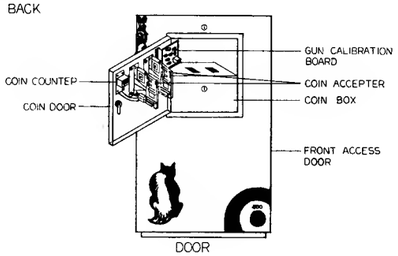
SECTION A-A

SIDE





FRONT



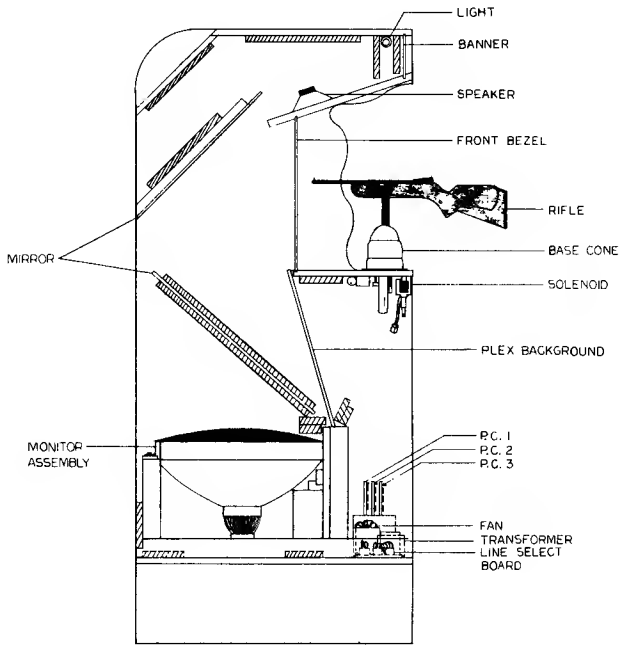
DOOR

TITLE
GAME TREE
FINAL ASSEMBLY

PROJECT SUPPORT ENGINEERING 760 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 738-8860	TOP ASSY.
	NEXT ASSY.
DRAWING NO	SCALE N/A

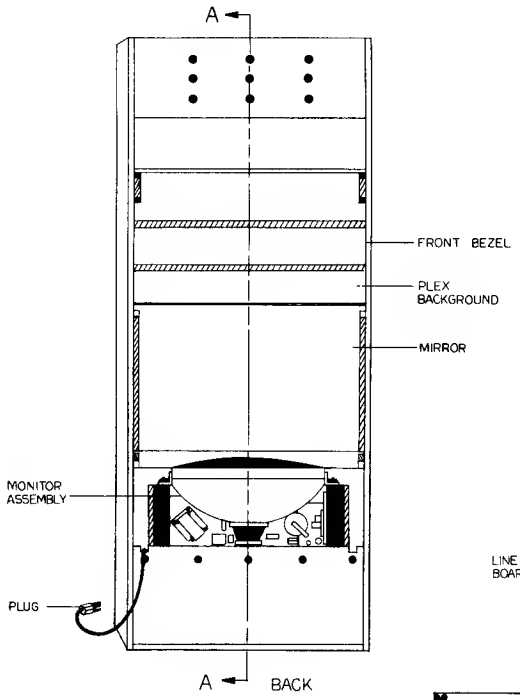
	APPROVED	INT.	DATE
DRAWN	J		10/77
CHECKED			
DESIGNER			
PROJ. ENG.			
SH. 1 OF 1			

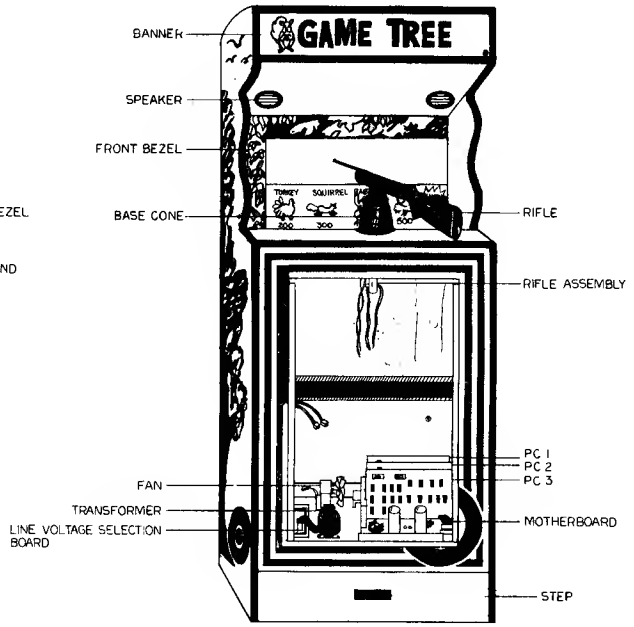
REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL



SECTION A-A

SIDE





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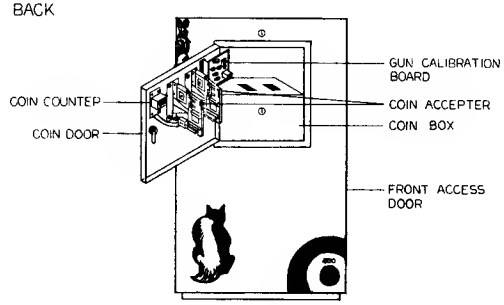
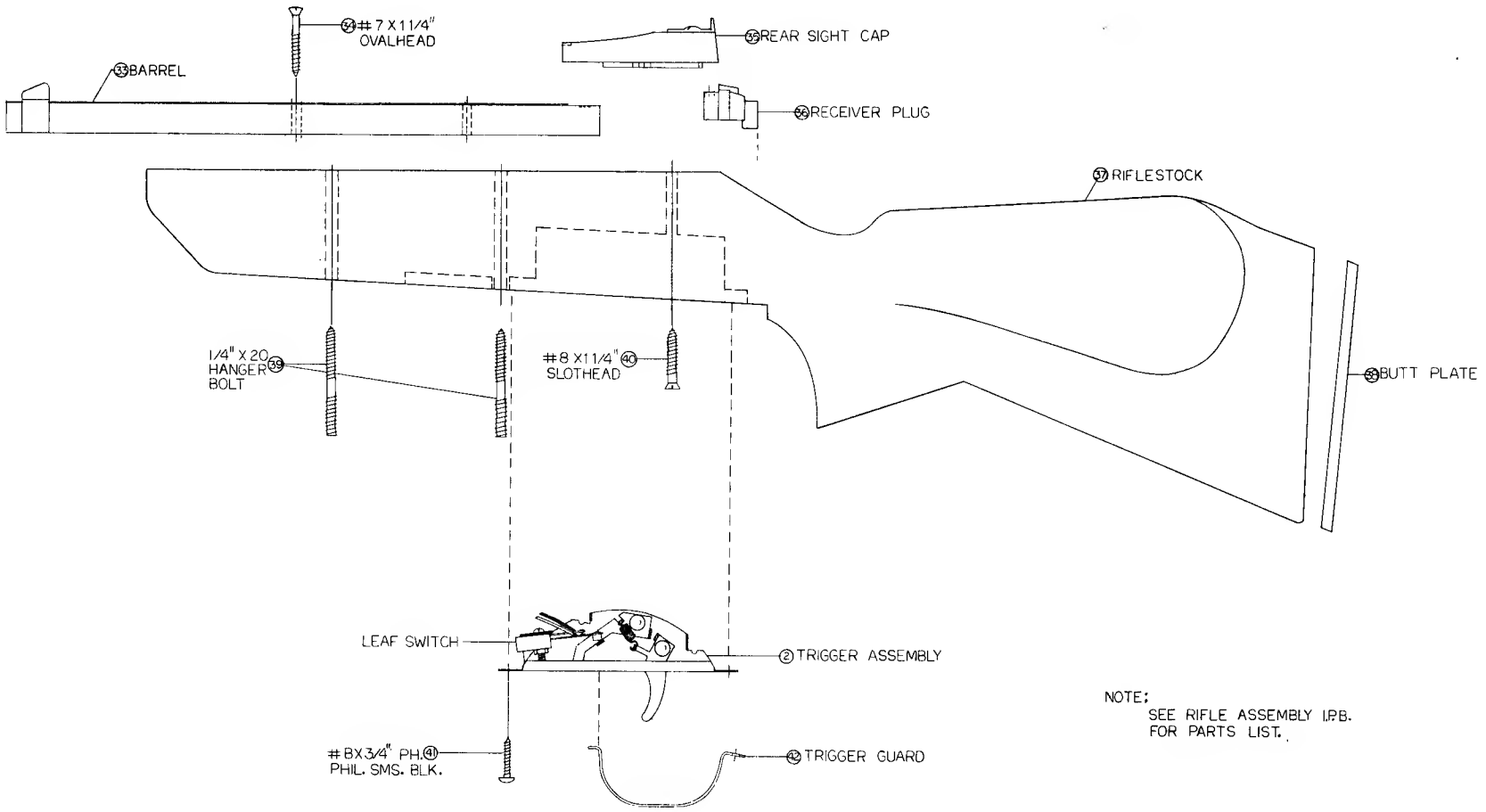


DOOR

PSE	TITLE: GAME TREE FINAL ASSEMBLY		
PROJECT SUPPORT ENGINEERING, 760 NORTH MARY AVENUE, SUNNYVALE, CALIFORNIA 94086, PHONE: (408) 738-8660	TOP ASSY.	APPROVED	INT. DATE
	NEXT ASSY.	DRAWN	8 11/77
		CHECKED	
		DESIGNER	
DRAWING NO	SCALE N/A	PROJ. ENG.	
		SH. 1 OF 1	

REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL

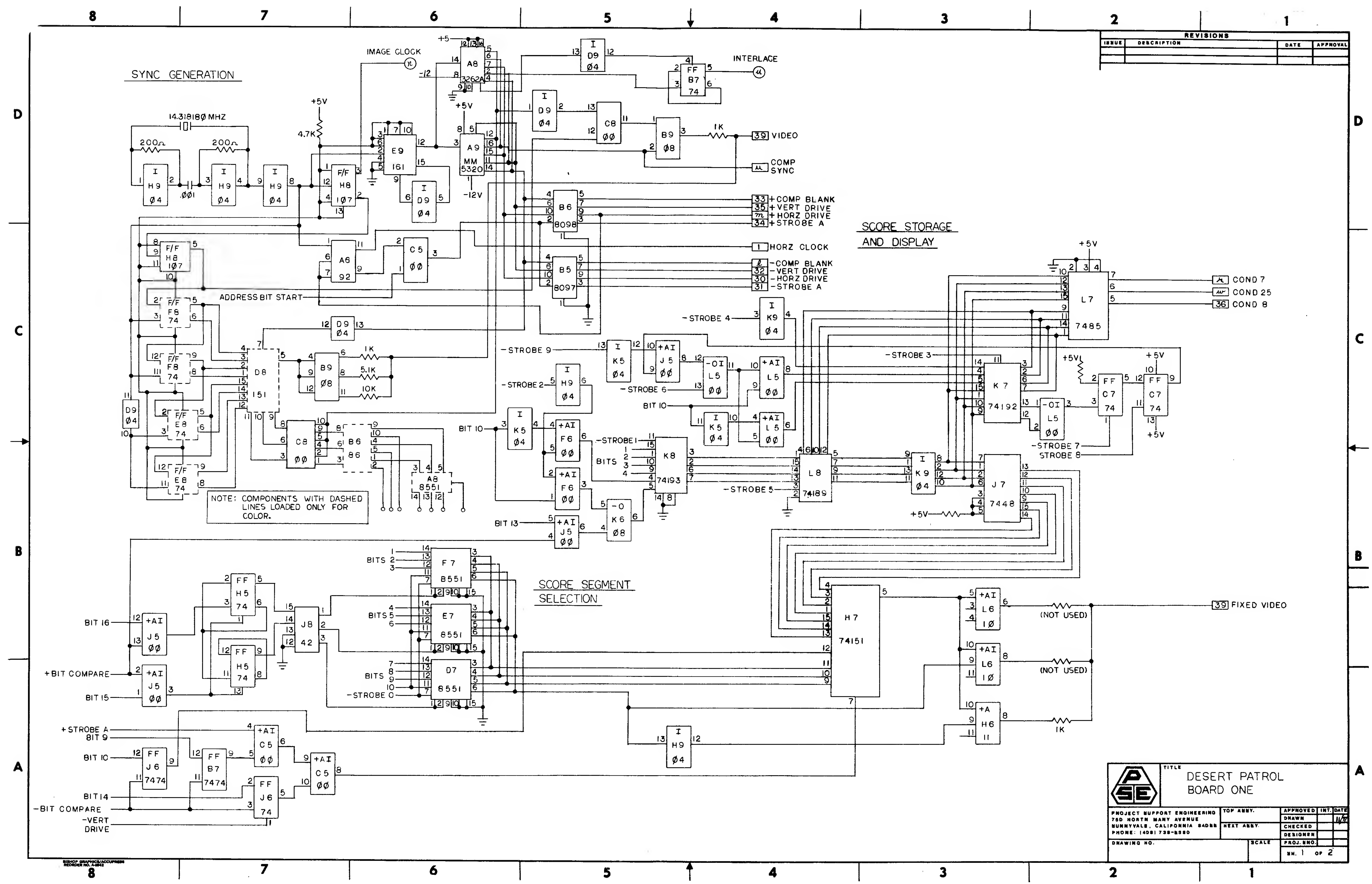


NOTE;
SEE RIFLE ASSEMBLY I.P.B.
FOR PARTS LIST.

TITLE
GAME TREE
RIFLE ASSEMBLY

PROJECT SUPPORT ENGINEERING
750 NORTH MARY AVENUE
SUNNYVALE, CALIFORNIA 94086
PHONE (408) 739-8550

TOP ASSY.		APPROVED	INT DATE
NEXT ASSY.		DRAWN	S 12/77
		CHECKED	
		DESIGNER	
DRAWING NO.	SCALE 1/1	PROJ. ENG.	
		SH. 1 OF 1	


SYNC GENERATION
14.318180 MHZ
IMAGE CLOCK
INTERLACE
VIDEO
COMP SYNC
+COMP BLANK
+VERT DRIVE
+HORZ DRIVE
+STROBE A
HORZ CLOCK
-COMP BLANK
-VERT DRIVE
-HORZ DRIVE
-STROBE A
ADDRESS BIT START
NOTE: COMPONENTS WITH DASHED LINES LOADED ONLY FOR COLOR.
SCORE STORAGE AND DISPLAY
COND 7
COND 25
COND 8
-STROBE 4
-STROBE 9
-STROBE 2
-STROBE 6
-STROBE 3
-STROBE 1
-STROBE 5
-STROBE 7
STROBE 8
BIT 10
BIT 13
BITS
SCORE SEGMENT SELECTION
FIXED VIDEO
(NOT USED)
BIT 16
+BIT COMPARE
BIT 15
+STROBE A
BIT 9
BIT 10
BIT 14
-BIT COMPARE
-VERT DRIVE
-STROBE 0
REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
TITLE
DESERT PATROL
BOARD ONE
PROJECT SUPPORT ENGINEERING
SUNNYVALE, CALIFORNIA
TOP ASSY.
NEXT ASSY.
APPROVED
INT.
DATE
DRAWN
CHECKED
DESIGNER
PROJ. ENG.
DRAWING NO.
SCALE
SH. 1 OF 2

PROGRAM CONTROL

BIT AND LINE COUNTERS

POWER SUPPLY

+5V POWER SUPPLY

+12 AND −12 POWER SUPPLY

REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL

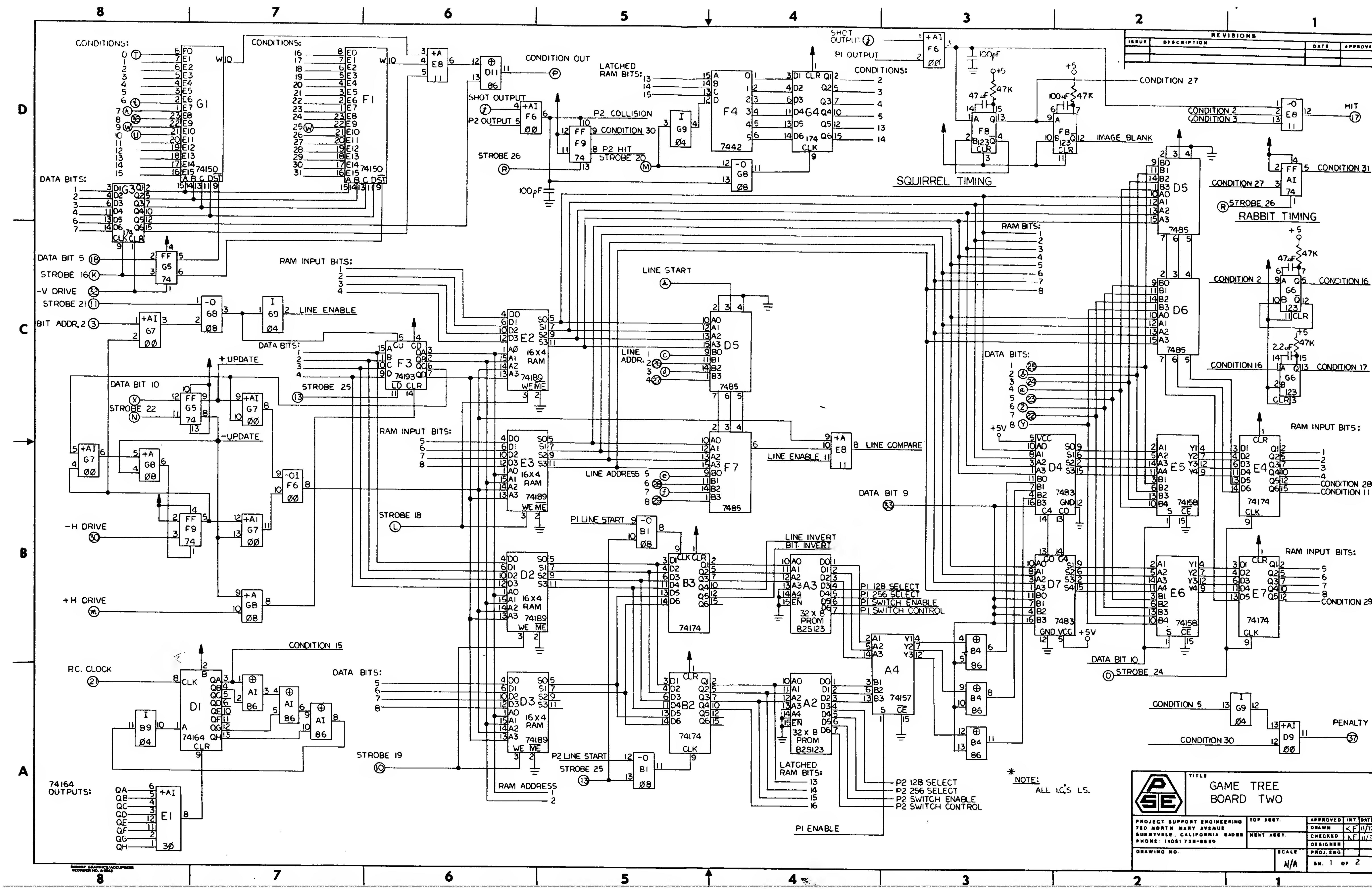
NOTES:
1. + 3 TO -3.5V
2. + 3 TO +3.5V
3. +6.5 TO + 7V
4. +4.75 TO + 5.25V
5. 16 VRMS
6. 8.5 VRMS

* TANTALUM

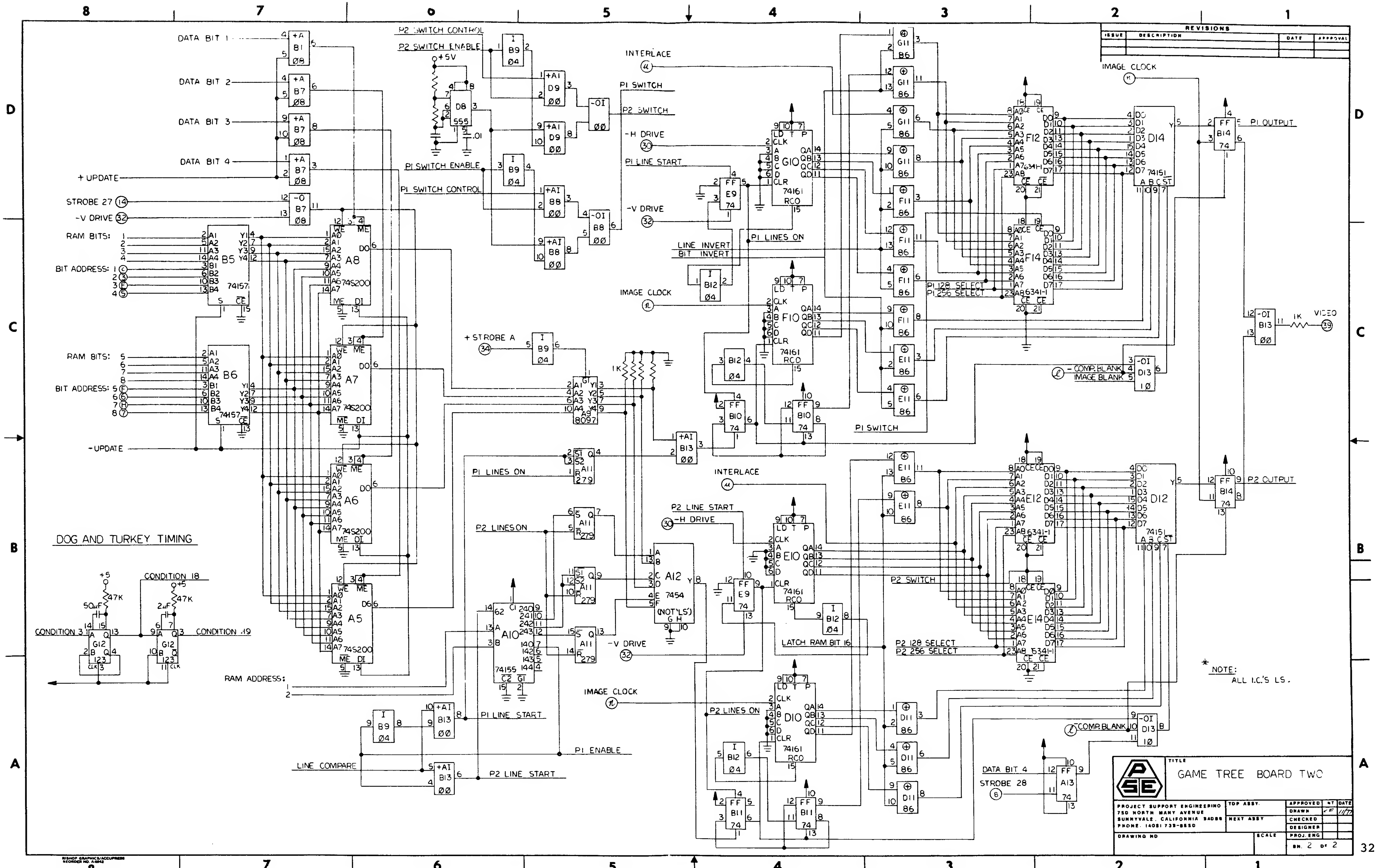
TITLE
DESERT PATROL & GAME TREE
BOARD ONE

PROJECT SUPPORT ENGINEERING
750 NORTH NARY AVENUE
SUNNYVALE, CALIFORNIA 94086
PHONE: (408) 739-8550

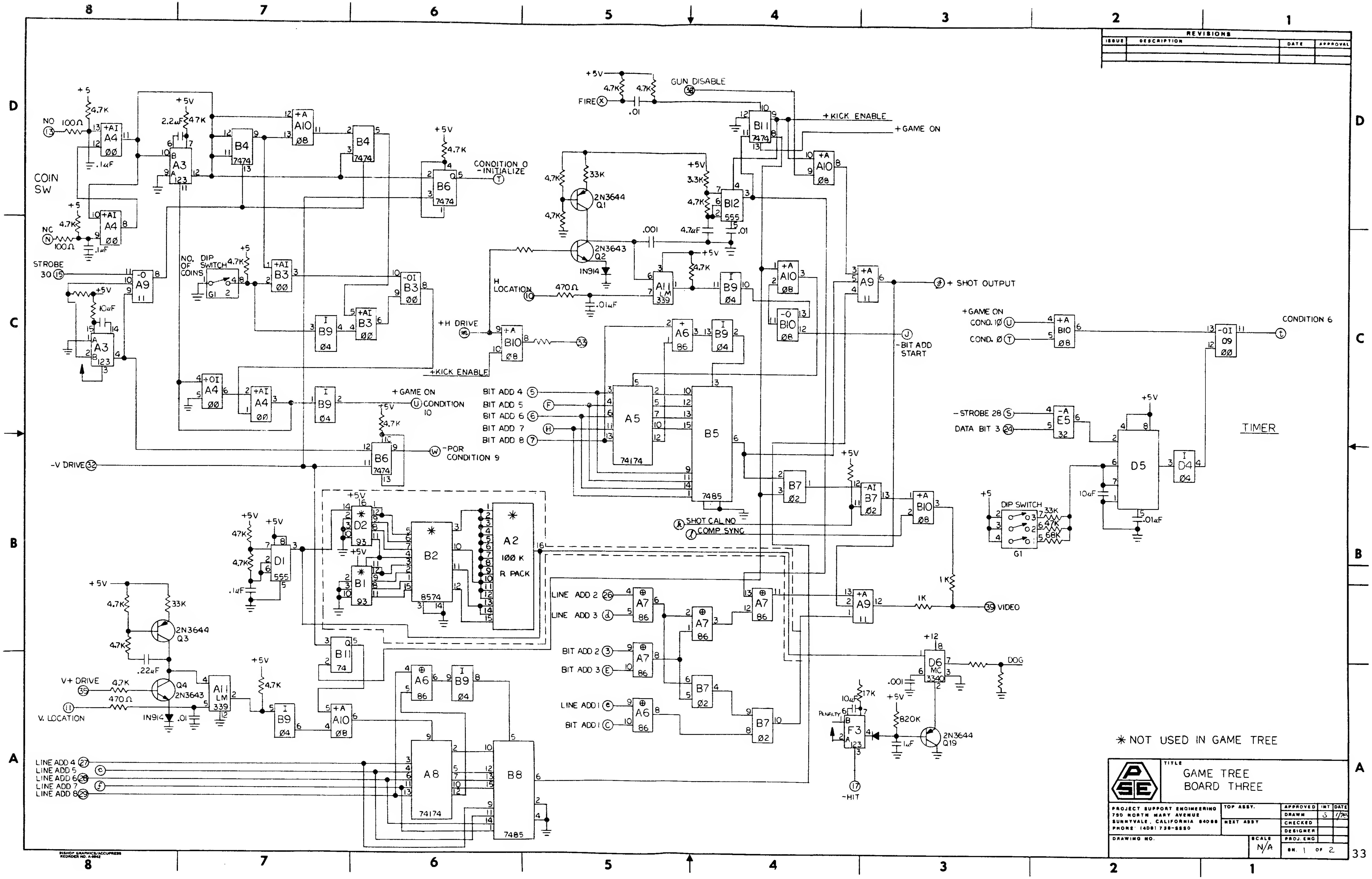
TOP ASSY.	APPROVED	INT.	DATE
	DRAWN		11/77
NEXT ASSY.	CHECKED		
	DESIGNER		
DRAWING NO.	SCALE	PROJ. ENG.	
		SH. 2 OF 2	



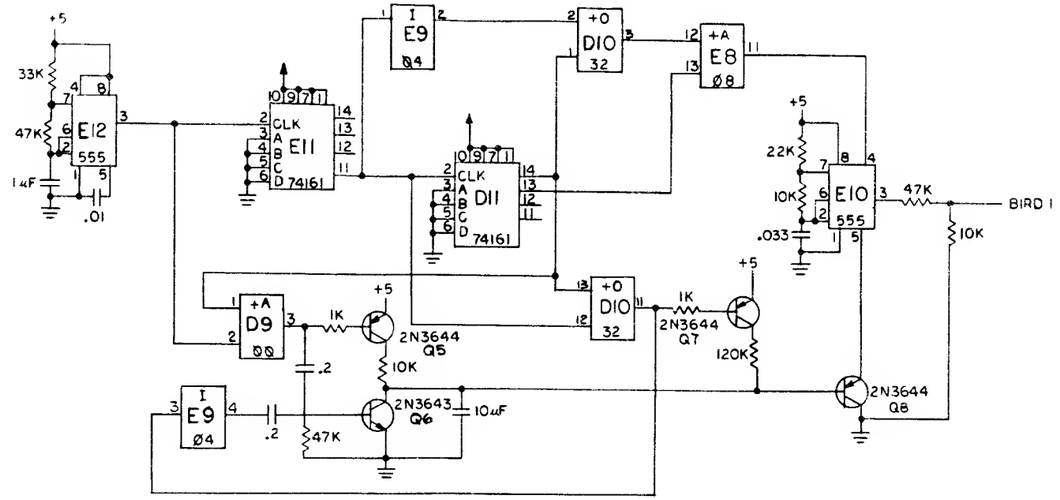
CONDITIONS:
DATA BITS:
74150
74174
CONDITION OUT
SHOT OUTPUT
P2 OUTPUT
P2 COLLISION
CONDITION 30
P2 HIT
STROBE 20
STROBE 26
LATCHED RAM BITS:
7442
P1 OUTPUT
CONDITION 27
SQUIRREL TIMING
IMAGE BLANK
HIT
CONDITION 31
RABBIT TIMING
RAM BITS:
RAM INPUT BITS:
LINE ENABLE
LINE START
LINE ADDR.
7485
16X4 RAM
74189
74193
+UPDATE
-UPDATE
DATA BIT 10
STROBE 22
DATA BIT 5
STROBE 16
-V DRIVE
STROBE 21
BIT ADDR. 2
-H DRIVE
+H DRIVE
LINE COMPARE
LINE ADDRESS
STROBE 18
P1 LINE START
LINE INVERT
BIT INVERT
32 X 8 PROM
82S123
P1 128 SELECT
P1 256 SELECT
P1 SWITCH ENABLE
P1 SWITCH CONTROL
74157
7483
74158
DATA BIT 9
CONDITION 28
CONDITION 11
CONDITION 29
STROBE 24
CONDITION 5
PENALTY
R.C. CLOCK
CONDITION 15
74164
74164 OUTPUTS:
STROBE 19
P2 LINE START
STROBE 25
RAM ADDRESS
P2 128 SELECT
P2 256 SELECT
P2 SWITCH ENABLE
P2 SWITCH CONTROL
P1 ENABLE
NOTE: ALL I.C.'S LS.
REVISIONS
GAME TREE BOARD TWO
PROJECT SUPPORT ENGINEERING
760 NORTH MARY AVENUE
SUNNYVALE, CALIFORNIA
PHONE: (408) 738-8660
DRAWING NO.
SCALE N/A
SH. 1 OF 2

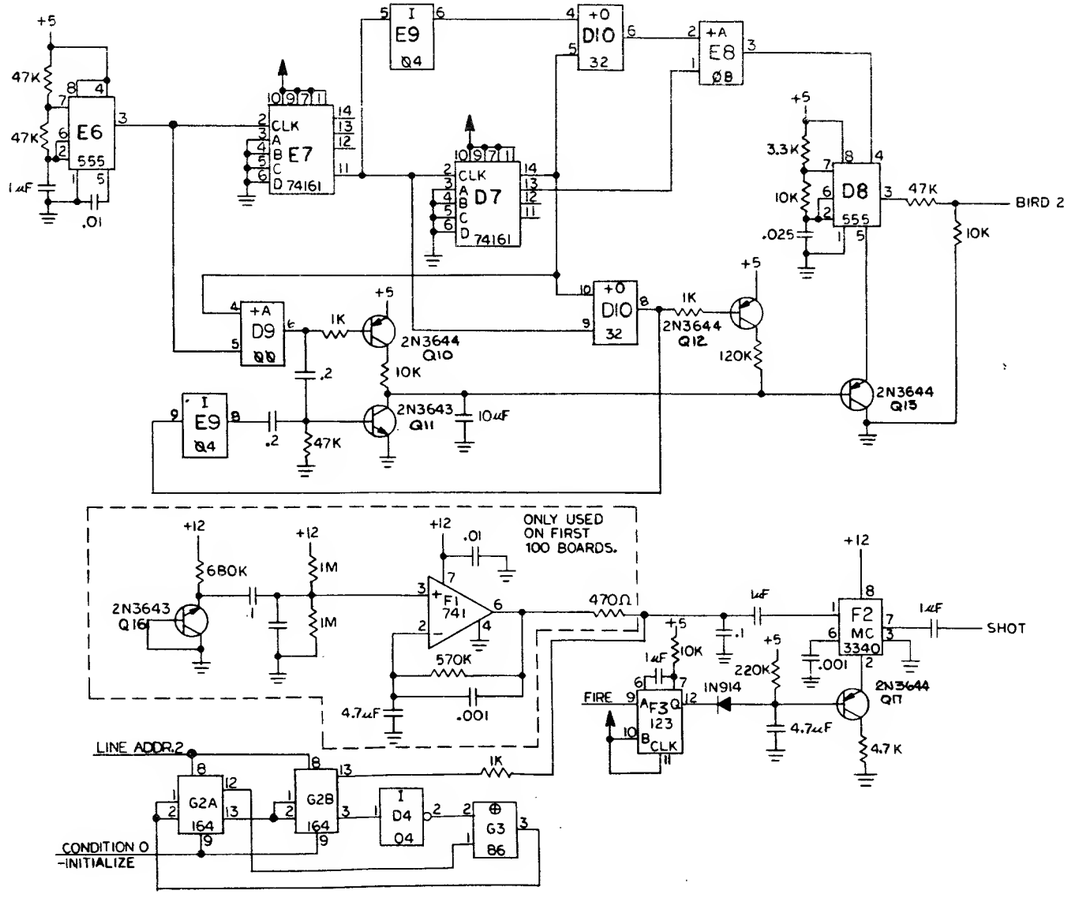


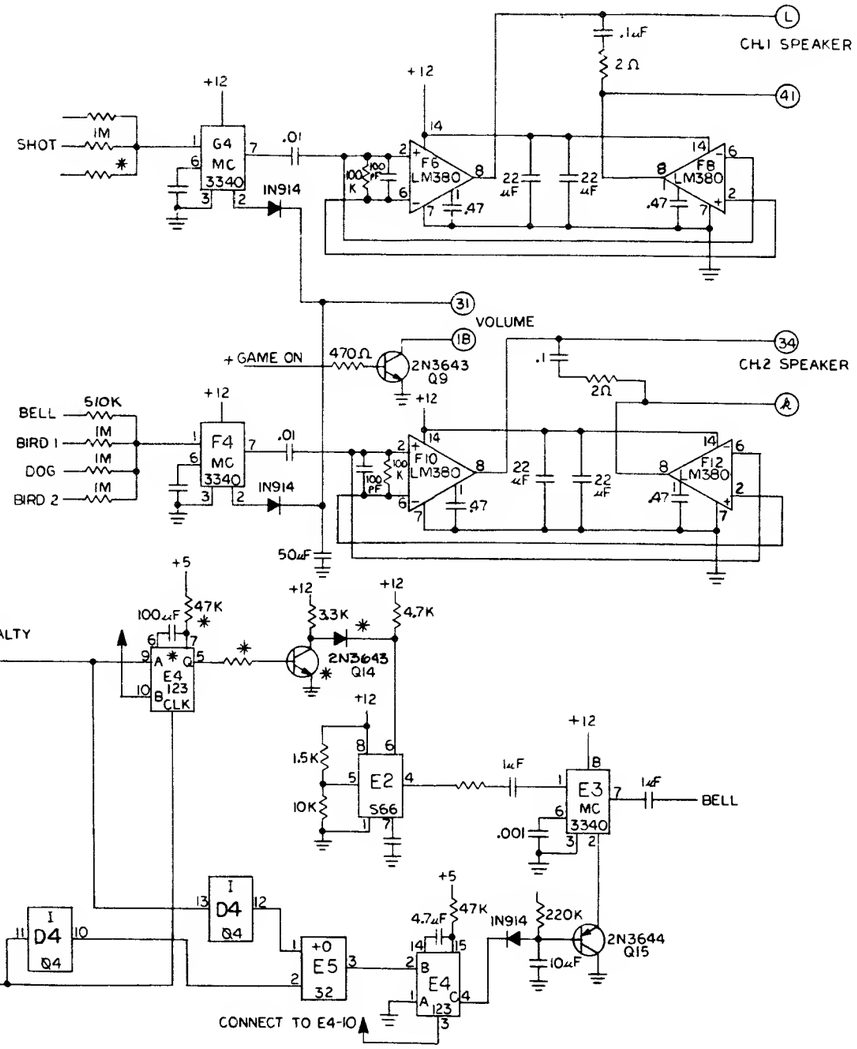
REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
DATA BIT 1
DATA BIT 2
DATA BIT 3
DATA BIT 4
+ UPDATE
STROBE 27
-V DRIVE
RAM BITS:
BIT ADDRESS:
74157
74S200
-UPDATE
P2 SWITCH CONTROL
P2 SWITCH ENABLE
+5V
555
P1 SWITCH ENABLE
P1 SWITCH CONTROL
INTERLACE
P1 SWITCH
P2 SWITCH
-H DRIVE
P1 LINE START
-V DRIVE
74161
LINE INVERT
BIT INVERT
P1 LINES ON
IMAGE CLOCK
+STROBE A
8097
(NOT 'LS')
7454
P1 LINES ON
P2 LINESON
P2 LINE START
LATCH RAM BIT 16
P2 LINES ON
P1 SWITCH
P2 SWITCH
P1 128 SELECT
P1 256 SELECT
P2 128 SELECT
P2 256 SELECT
6341-1
74151
P1 OUTPUT
P2 OUTPUT
VIDEO
1K
-COMP. BLANK
IMAGE BLANK
COMP. BLANK
DOG AND TURKEY TIMING
CONDITION 18
CONDITION 3
CONDITION 19
50μF
2μF
47K
RAM ADDRESS:
P1 LINE START
P1 ENABLE
LINE COMPARE
P2 LINE START
DATA BIT 4
STROBE 28
* NOTE: ALL I.C.'S LS.
TITLE
GAME TREE BOARD TWO
PROJECT SUPPORT ENGINEERING
750 NORTH MARY AVENUE
SUNNYVALE, CALIFORNIA 94086
PHONE: (408) 735-8550
TOP ASSY.
NEXT ASSY
DRAWING NO
SCALE
APPROVED
DRAWN
CHECKED
DESIGNER
PROJ. ENG
SH. 2 OF 2


REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
COIN SW
NO
NC
STROBE 30
NO. OF COINS
DIP SWITCH
CONDITION 0 -INITIALIZE
+H DRIVE
+KICK ENABLE
+GAME ON
CONDITION 10
-POR CONDITION 9
-V DRIVE
FIRE
GUN DISABLE
+KICK ENABLE
+GAME ON
2N3644 Q1
2N3643 Q2
H LOCATION
+ SHOT OUTPUT
-BIT ADD START
BIT ADD 4
BIT ADD 5
BIT ADD 6
BIT ADD 7
BIT ADD 8
SHOT CAL NO
COMP SYNC
+GAME ON
COND. 10
COND. 0
CONDITION 6
-STROBE 28
DATA BIT 3
TIMER
DIP SWITCH
100 K R PACK
LINE ADD 2
LINE ADD 3
BIT ADD 2
BIT ADD 3
LINE ADD 1
BIT ADD 1
VIDEO
DOG
2N3644 Q3
2N3643 Q4
V+ DRIVE
V. LOCATION
PENALTY
-HIT
2N3644 Q19
LINE ADD 4
LINE ADD 5
LINE ADD 6
LINE ADD 7
LINE ADD 8
✳ NOT USED IN GAME TREE
TITLE
GAME TREE BOARD THREE
PROJECT SUPPORT ENGINEERING
790 NORTH MARY AVENUE
SUNNYVALE, CALIFORNIA 94086
TOP ASSY.
NEXT ASSY
DRAWING NO.
SCALE N/A
SH. 1 OF 2
APPROVED
DRAWN
CHECKED
DESIGNER
PROJ. ENG

REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL
A	REVISIONS	1/78	





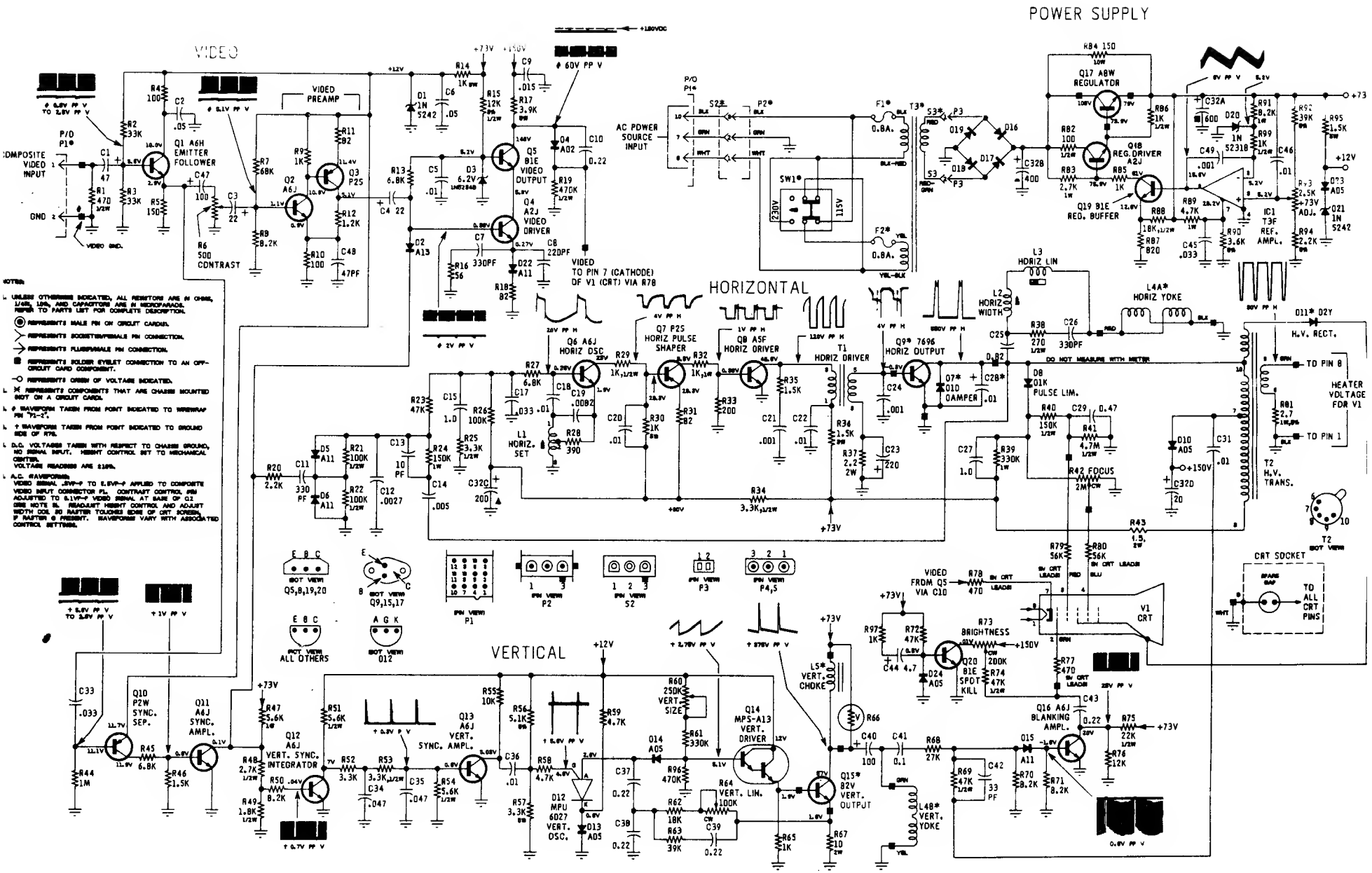


* NOT USED FOR GAME TREE

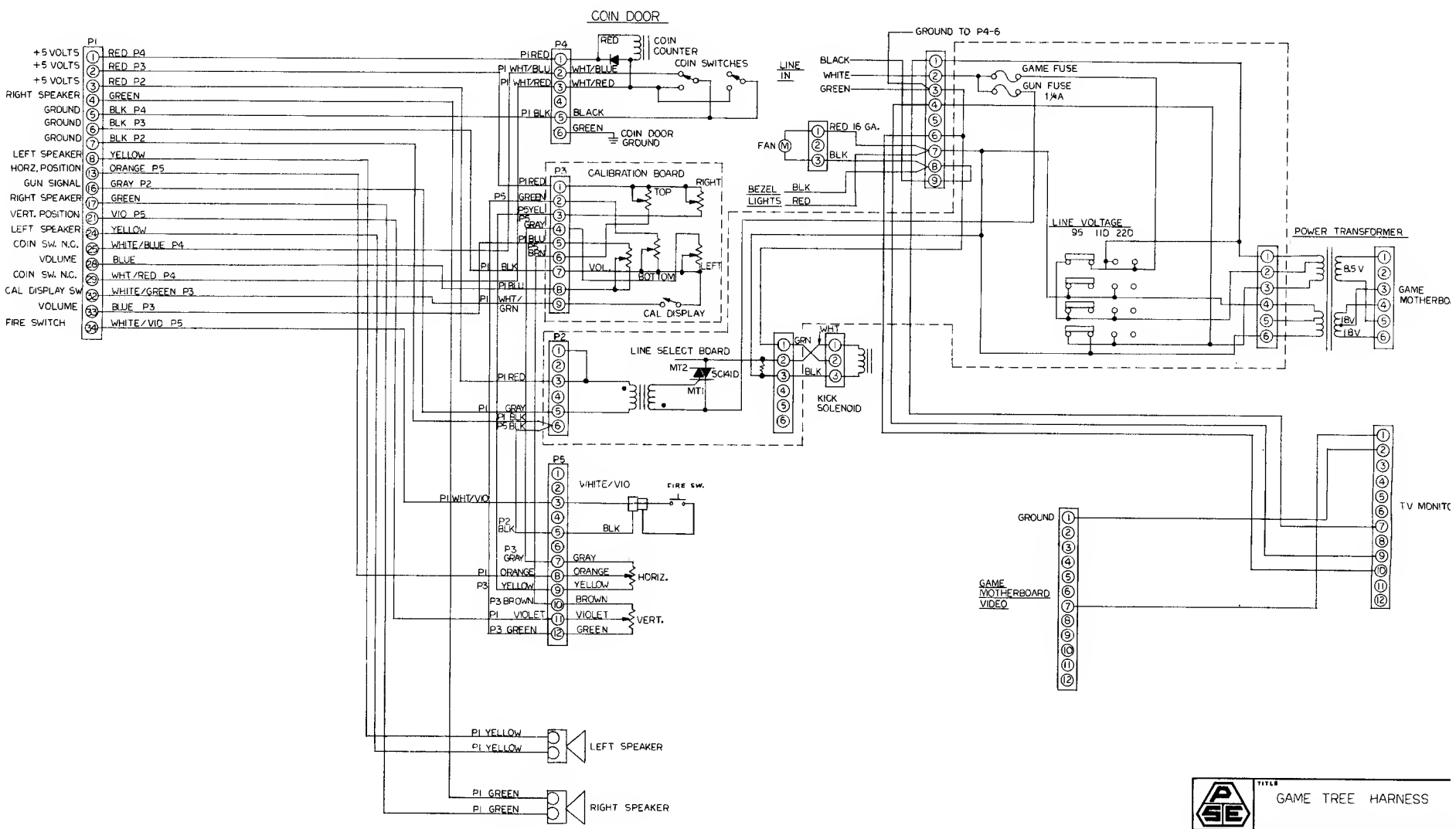
PSE

TITLE
GAME TREE
BOARD THREE

PROJECT SUPPORT ENGINEERING 750 NORTH MARY AVENUE SUNNYVALE, CALIFORNIA 94086 PHONE: (408) 735-5550	TOP ASSY.	APPROVED	INT.	DATE
		DRAWN	JS	10/77
	SHEET ASSY.	CHECKED		
		DESIGNER		
DRAWING NO.	SCALE	PROJ. ENG.		
		SH. 2 OF 2		



M5000–155, M7000–155 – Diagram Schematic



REVISIONS			
ISSUE	DESCRIPTION	DATE	AP

TITLE: GAME TREE HARNESS

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780 NORTH MARY AVENUE
SUNNYVALE, CALIFORNIA 94086
PHONE: (408) 735-8850

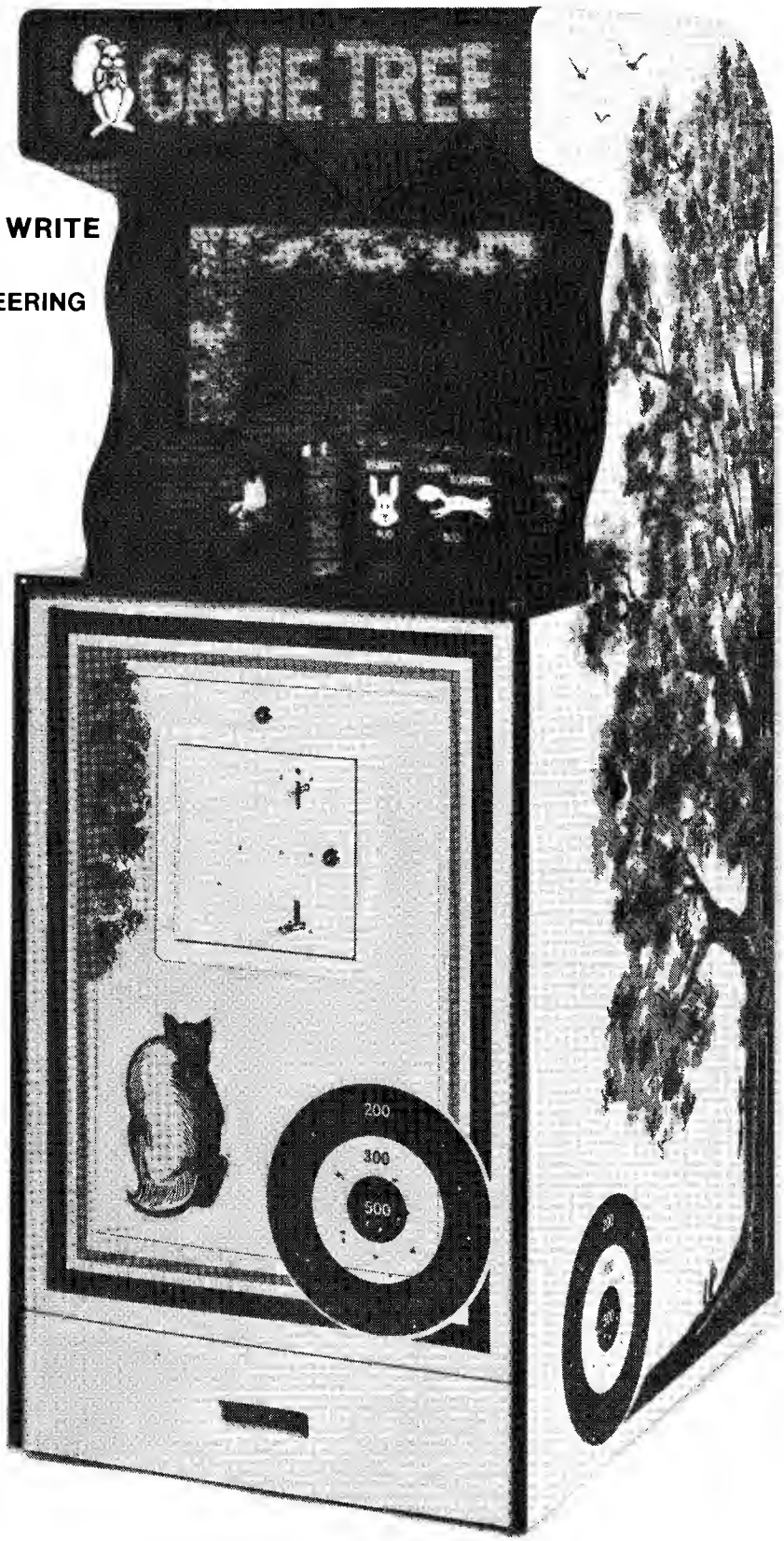
TOP ASSY.
NEXT ASSY

APPROVED
DRAWN
CHECKED
DESIGNED
PROJ. ENG.

DRAWING NO

SCALE N/A

SH. 1 OF 1



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SUNNYVALE, CA. 94086

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PSE

TRI-STATE Hex Buffers

General Description

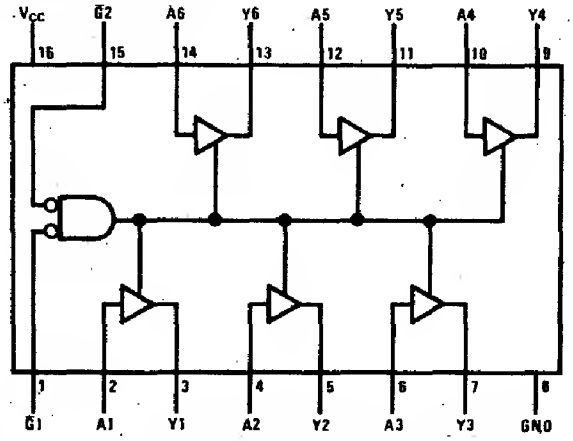
These devices provide six, two-input buffers in each package. Both the standard (7400 compatible) TTL technology, and the "true tenth-power" (74L compatible) low power versions are available for each of the four types. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present the true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all six control lines for TRI-STATE enable are common in a single line. On the 97 and 98 versions, four buffers are enabled from a common line, and the other two buffers from a separate common line. In all cases, the outputs are placed in the TRI-STATE condition by applying a high logic level to the control pins. With either the standard TTL or the low power versions of these circuits, it is possible to connect over 100 like devices to a common bus line and still have adequate drive capability.

Features

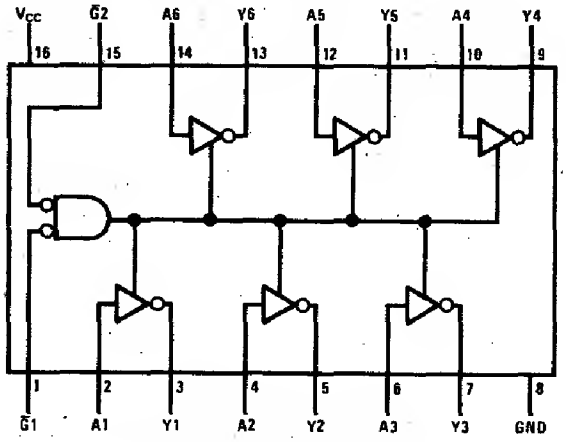
TYPE	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAY
95, 97	325 mW	12 ns
L95, L97	20 mW	34 ns
96, 98	295 mW	11 ns
L96, L98	15 mW	31 ns

- Pin equivalent to DM54365 (95), DM54366 (96), DM54367 (97), DM54368 (98)

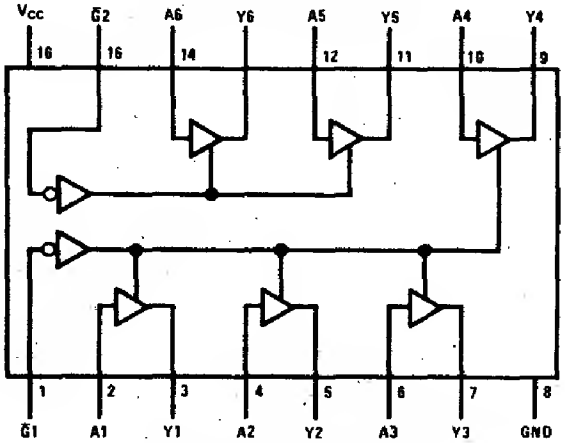
Connection Diagrams



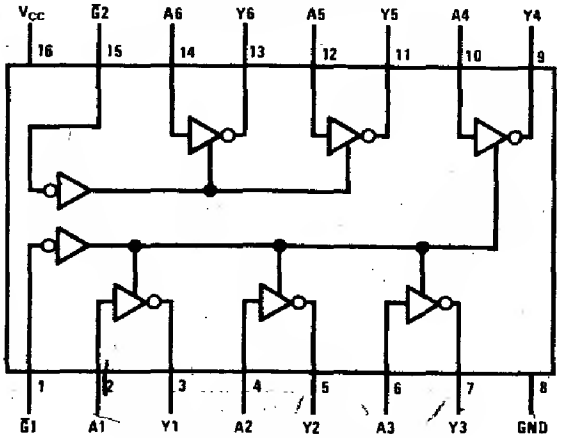
7095(J), (W); 8095(J), (N), (W);
70L95/80L95(J), (N), (W)



7096(J), (W); 8096(J), (N), (W);
70L96/80L96(J), (N), (W)



7097(J), (W); 8097(J), (N), (W);
70L97/80L97(J), (N), (W)



7098(J), (W); 8098(J), (N), (W);
70L98/80L98(J), (N), (W)

Truth Tables (Each Driver)

95, L95

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

96, L96

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	L
L	L	L	H

97, L97

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

98, L98

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

Magnitude Comparators

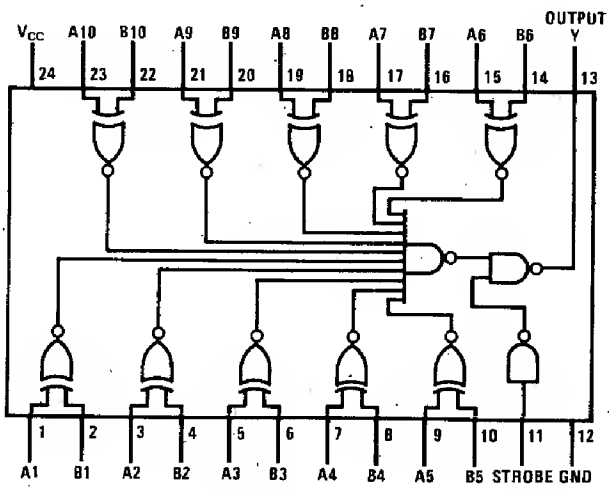
General Description

These devices offer comparisons to determine equality between two binary words. The DM7130/DM8130 compares two ten-bit words, and the DM7160/DM8160 compares two six-bit words. A strobe override is provided on both devices. When the strobe is taken to a high logic level, the output is forced to a high logic level. The devices also feature open collector outputs for expansion.

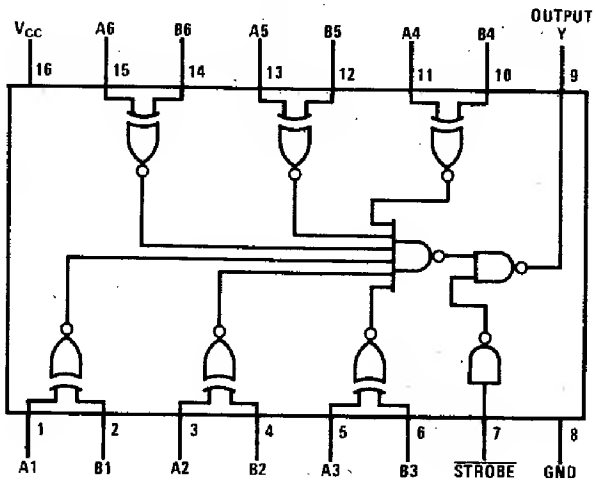
Features

- Typical propagation delay 21 ns
- Typical power dissipation
  - DM7130/8130 240 mW
  - DM7160/8160 205 mW
- Open-collector outputs for expansion

Connection Diagrams



7130(J), (F); 8130(J), (N), (F),



7160(J), (W); 8160(J), (N), (W)

Truth Table

CONDITION	$\overline{\text{STROBE}}$ S	OUTPUT Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

TRI-STATE 4-Bit D Type Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

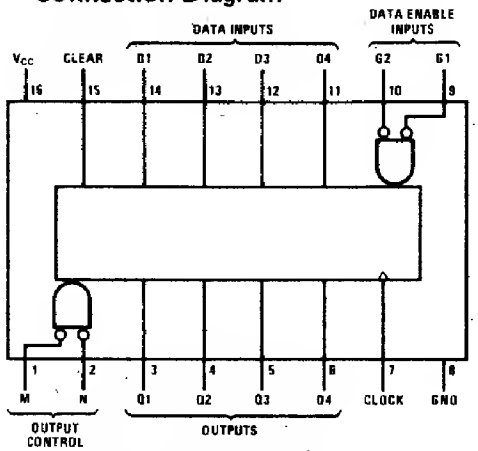
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL FREQUENCY	TYPICAL POWER DISSIPATION
7551/8551	18 ns	30 MHz	250 mW
75L51/85L51	59 ns	15 MHz	27.5 mW

Connection Diagram



7551(J), (W); 8551(J), (N), (W);
75L51/85L51(J), (N), (W)

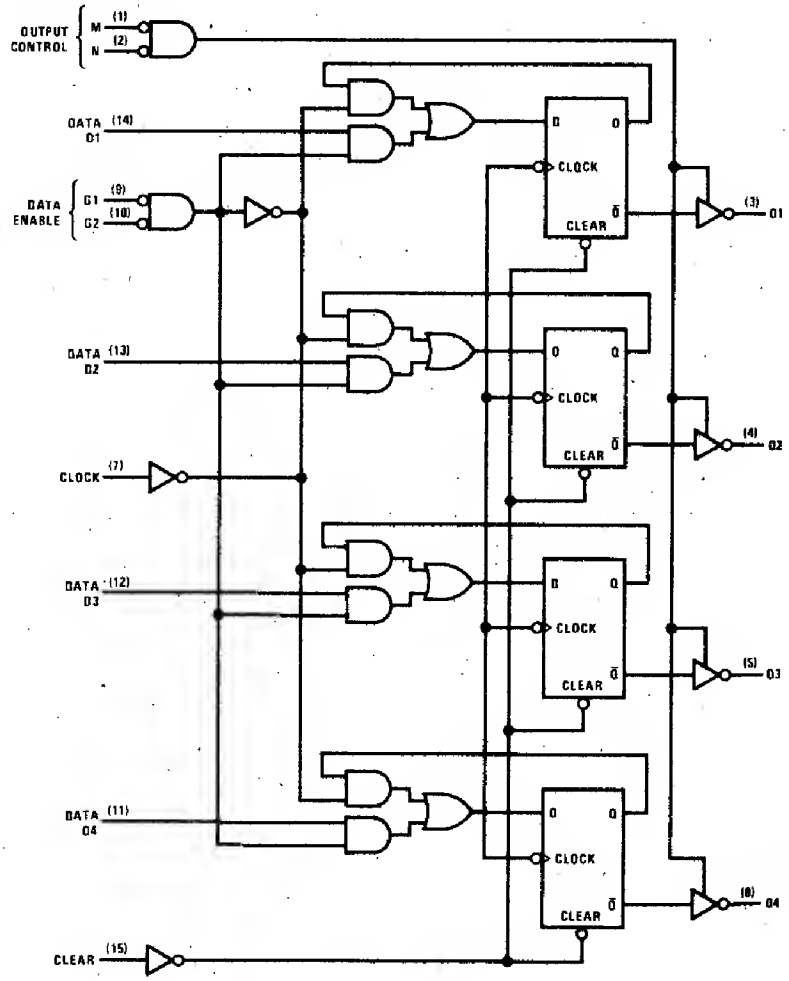
Truth Table

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Logic Diagram



TRI-STATE 8-Bit Latches

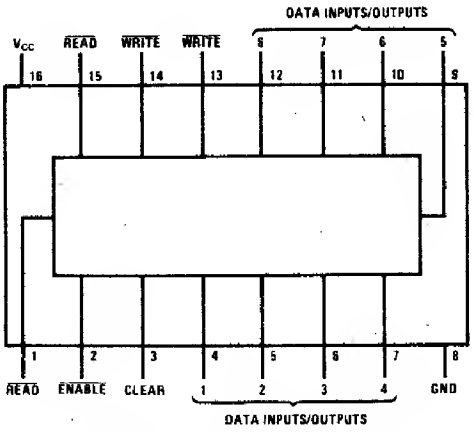
General Description

By utilizing TRI-STATE circuitry on the outputs, the inputs and outputs can be accessed on the same pins, and these circuits provide eight separate $\overline{R}$-$\overline{S}$ latches in the popular 16-pin package. While in the high-impedance state, the inputs and outputs are disabled and no information can be entered. When both $\overline{WRITE}$ inputs are brought to a low logic level, the outputs are disabled and new information may be entered at the inputs. When a low logic level is applied to both $\overline{READ}$ inputs, and a high logic level to both $\overline{WRITE}$ inputs, the inputs are rendered inactive and data may be read from the outputs.

Features

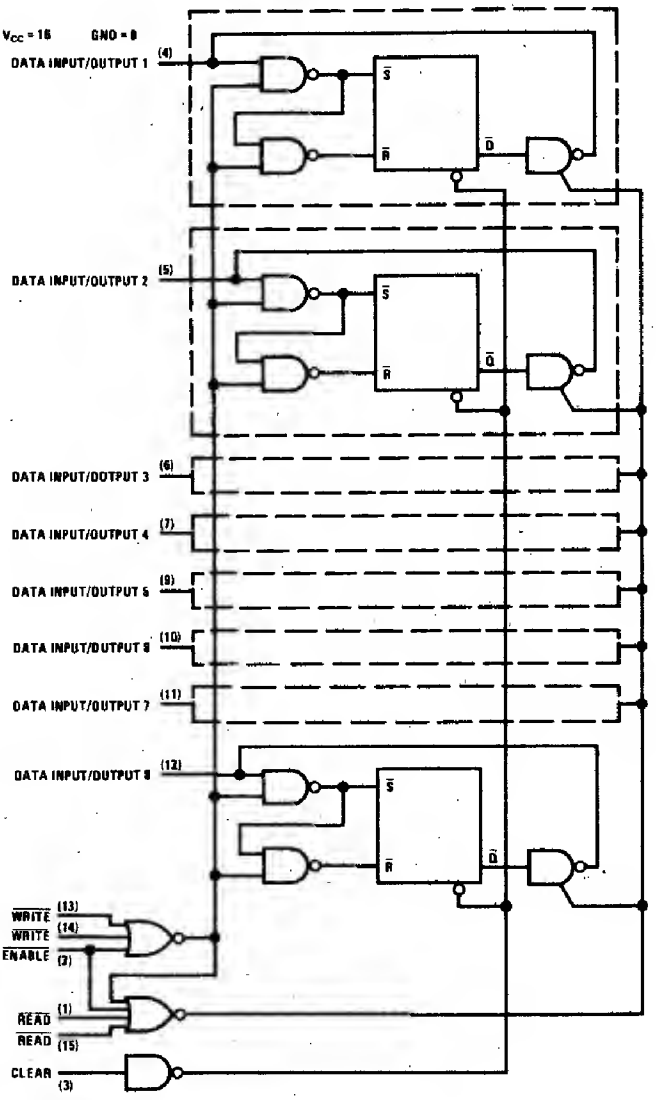
- TRI-STATE I/O pins
- 8 latches in popular 16-pin package
- Typical propagation delay—22 ns

Connection Diagram



7553(J), (W); 8553(J), (N), (W)

Logic Diagram



Truth Table

CLEAR	$\overline{ENABLE}$	$\overline{READ}$*	$\overline{WRITE}$**	OPERATION	STATE OF BUS
H	L	L	H	Enter L	L
H	L	L	L	Enter L	Hi-Z
L	X	H	H	Do Nothing	Hi-Z
L	H	X	X	Do Nothing	Hi-Z
L	L	X	L	Write	H or L***
L	L	L	H	Read	H or L***

*Both Read Inputs
**Both Write Inputs
***Depends on State of Latch

TRI-STATE 1024-Bit Field Programmable Read Only Memories

General Description

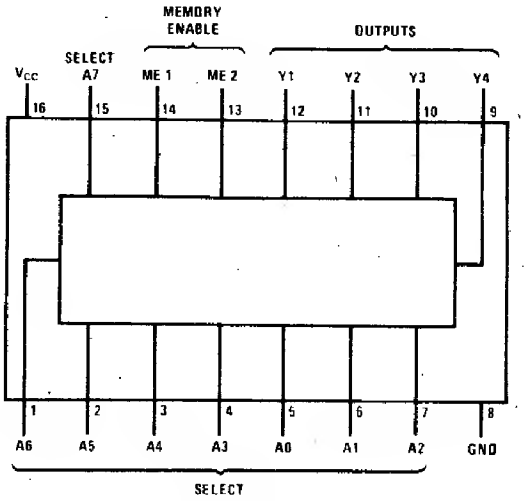
The DM7574/DM8574 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs go to the high impedance state. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7574/DM8574 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 10V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer problems.

Features

- Pin compatible with SN54187/SN74187
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

Connection Diagram



7574(J); 8574(J), (N)

Logic Diagram